Data Acquisition System for Belle II

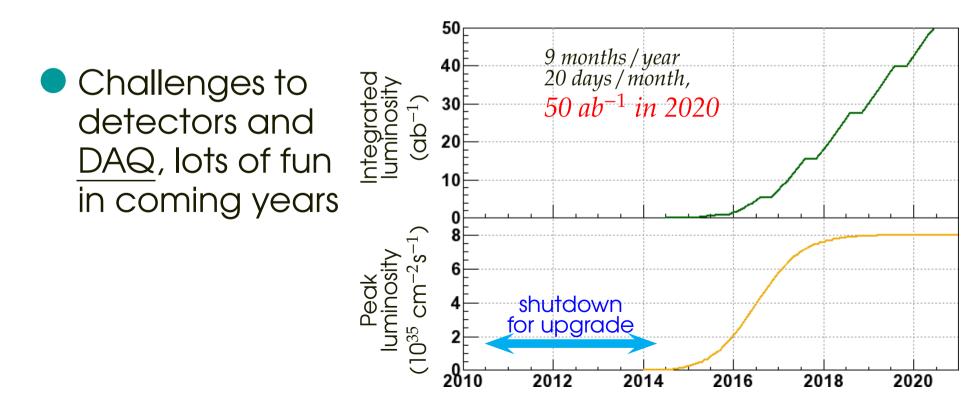
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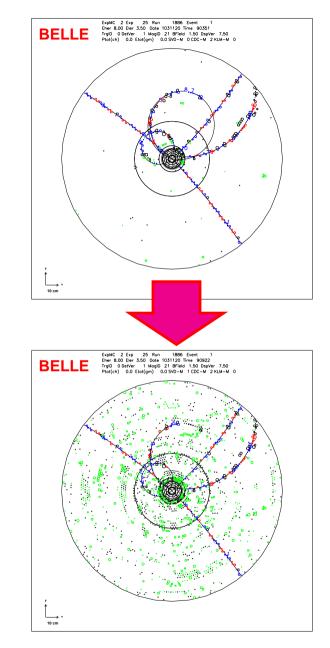
Belle II at SuperKEKB

- KEKB/Belle has been extremely successful, yet ...
- Flavor physics (*B*, *D* & τ) with 50 ab⁻¹ (~50 billion of each) to identify new physics (synergy with direct searches at LHC)
 - 400 collaborators from Asia, Europe and US
 - Project approved this year, funding has started U

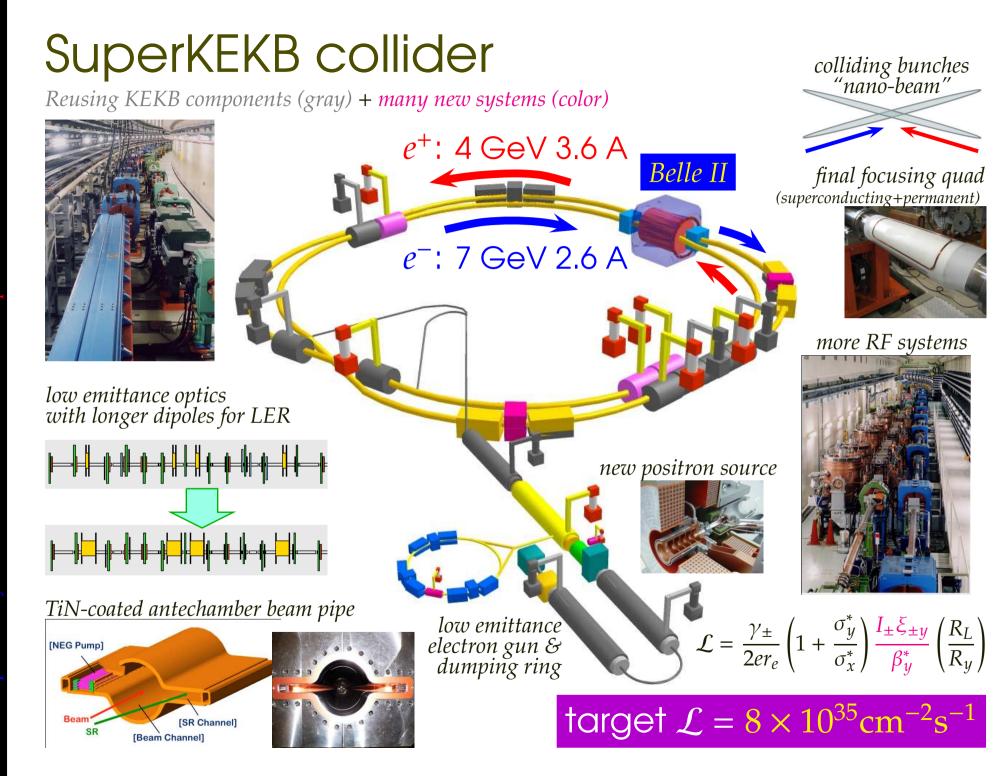


Wishes & Challenges

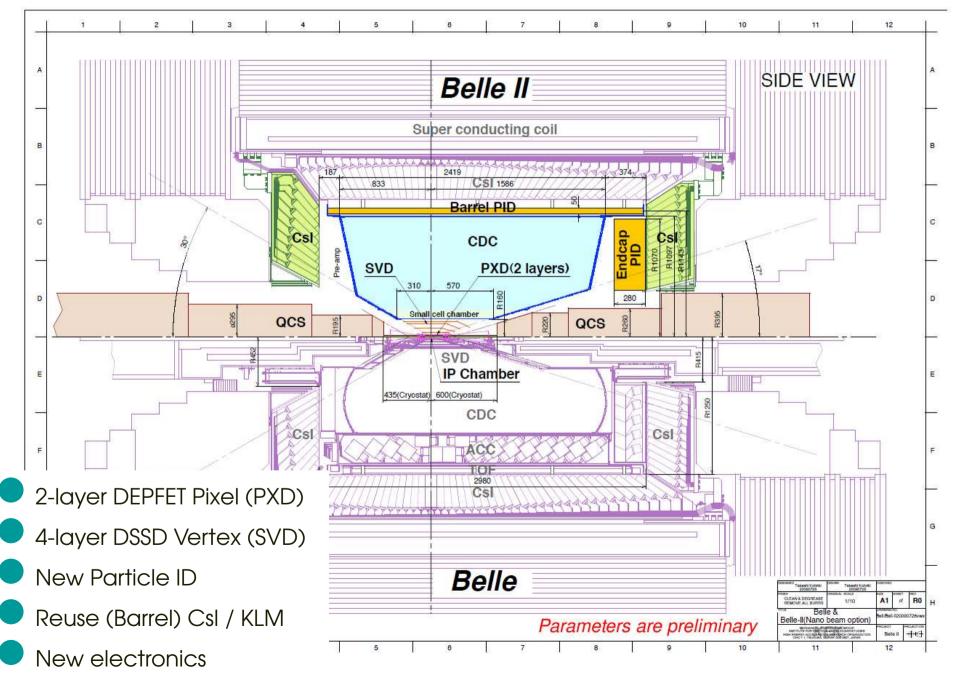
- For a higher luminosity
 - More beam background (~20 times)
 - Higher trigger rate (~40 times)
 - More radiation
- To improve the detector
 - *Pixel detector (DEPFET)*
 - New particle ID system
 - *Finer granularity (more channels)*
 - *Faster electronics (shorter time window)*
- Other constrains
 - Limited human/funding resources
 - *Limited space (no hermeticity gain/loss)*
 - ~100% efficiency is required



an example with 20× noise hits

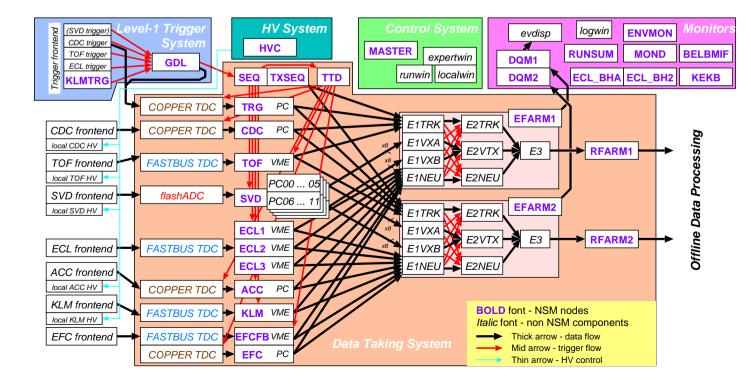


Belle II detector



Experiences at Belle I

- "Unified" readout system Q-to-T and multihit TDC
- Low trigger rate, up to 500 Hz, readout not pipelined
- 40 kB / event, 20 MB/s total rate,
 Point-to-point TCP connection for L3 trigger / event building
- Limited human resources, smoothly operated over 10 years

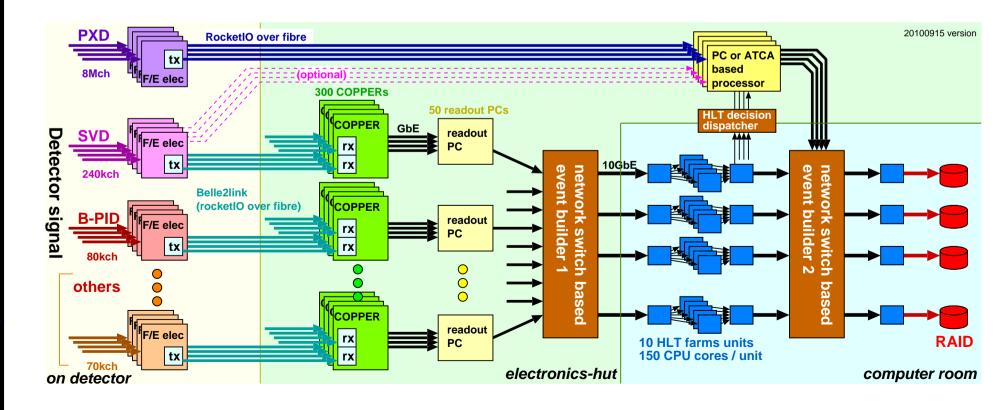


Belle II DAQ constraints

- 20 kHz nominal L1 trigger rate (40 times higher) ~1 kHz each of $b\overline{b}$, $c\overline{c}$, $\tau^+\tau^-$, >99% efficiency for $b\overline{b}$
- 5 μs L1 trigger latency (only twice longer) Limited by the APV25 readout of SVD
- 2ns beam bunch spacing (unchanged) Colliding bunch is not identified online, resolved in offline
- Huge data from Pixel detector Special handling, dominating the bandwidth
- Still huge data even without Pixel detector Fast optical transmission & network system, challenges to offline
- Limited human resources (unchanged :-<) Unification based on universal components (reusing Belle concepts)

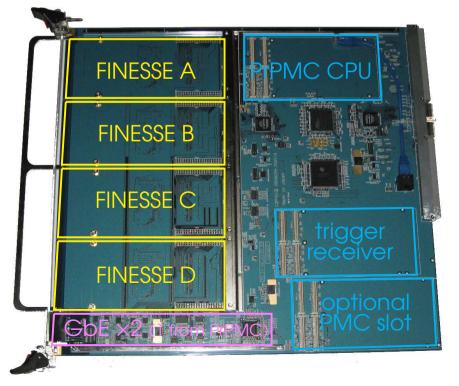
Belle II DAQ concept

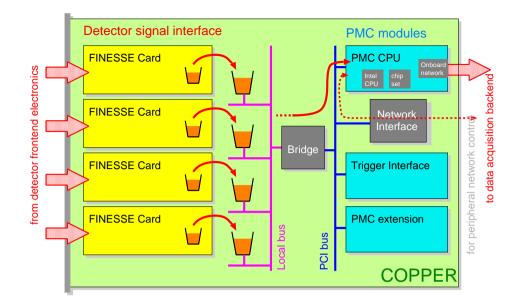
- Detector specific digitization + unified datalink
- Common receiving platform (COPPER) and GbE
- Network switch based 2-stage event building
- "Offline" reconstruction at high level trigger (HLT) farm
- PXD data as an additional dataflow



COPPER platform

- Modular structure
 4x FINESSE daughter cards,
 PrPMC CPU, trigger receiver
- Dedicated for readout 1MB FIFO per FINESSE, fast control signals





- Compact VME 9U board
 - COPPER2 designed in 2002,
 ~ 200 boards used in Belle,
 widely used at KEK & J-PARC
- COPPER3 board: revised in 2008 for next 10-year lifetime
- Limitations 32-bit 33 MHz PCIbus, PrPMC performance

PrPMC

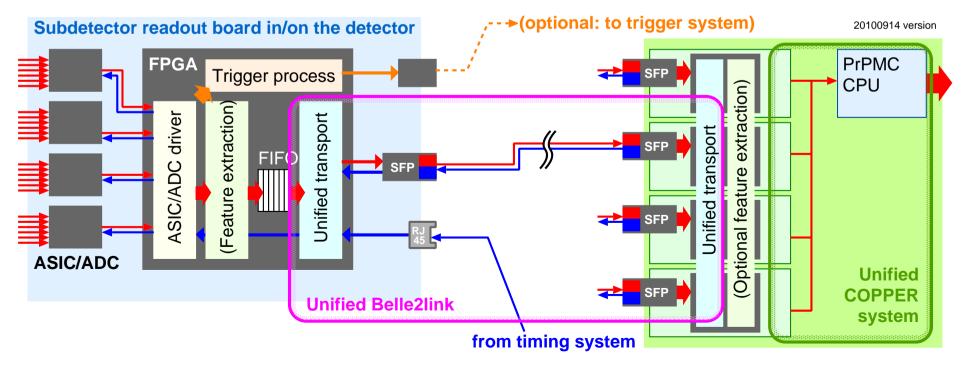
- Intel x86 CPU in a small PMC form factor
 - *Running Linux OS (RedHat, CentOS)*
- Pentium III 800MHz based PrPMC in Belle

Atom Z530 1.6 GHz based PrPMC for Belle II

- To be used for next 10 years
- Newly developed by the manufacturer who made COPPER
- Software and running environment resources developed for Belle
- New PrPMC under evaluation
 - Functionally OK
 - Tested at 40 kHz L1 trigger

Belle2link

- Frontend for CDC & PID are inside the detector, Serialized datalink to reduce the number of cable
- Unified datalink protocol on Xilinx RocketlO (GTP) from detector area to COPPER (~20m)
- Integrated timing system interface (LVDS)
- Two paths for their remote control (optical/LVDS)



FINESSE

- TDC FINESSE has been used in Belle (compatible to LeCroy FASTBUS TDC)
- Belle2link receiver FINESSE in Belle II
 - *Xilinx Virtex5-LXT FPGA (RocketIO GTP up to 3 Gbps)*
 - For most of the detector, FINESSE is just a receiver, bandwidth will never saturate
 - Feature extraction (DSP) for barrel-PID & endcap-KLM, raw sampling data transmitted over Belle2link

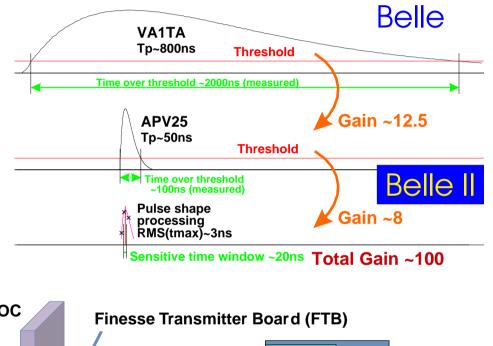


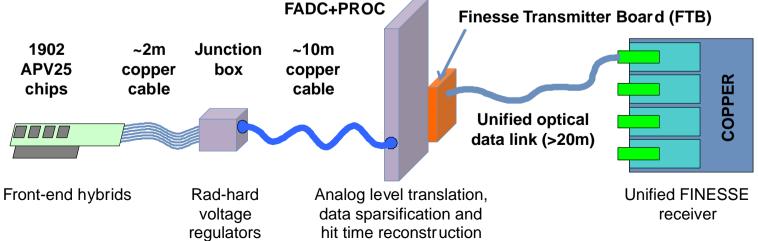
DSP Belle2link Receiver Prototype



SVD readout

- APV25: 6 sample readout & external pulse finding, timewise occupancy reduction makes it even more quiet than Belle
- Driven by 32MHz clock
 - 5μs buffer
 - 🗢 200 ns trigger interval
 - up to 5 triggers in pipeline
 - 27 μs to readout
 - **3**.5% deadtime at 30 kHz

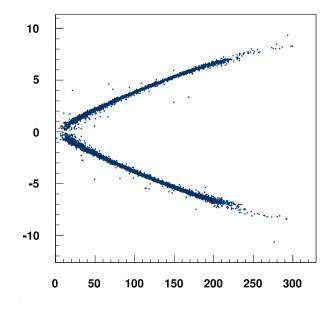




CDC readout

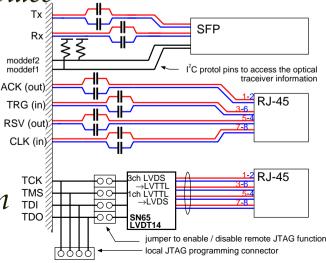
- FlashADC + FPGA-TDC(1GHz)
- Prototype readout board is ready with a test chamber (x-t curve)
- 48 ch per board, just behind the CDC endplate (inside detector) including preamp, ADC, FPGA, and optical transceiver
- Extracting the analog signal out of the detector is no more realistic due to the increase in the number of channel
- Trigger information also generated
- Radiation and maintenance could be an issue (similar worries on B- and E-PID)

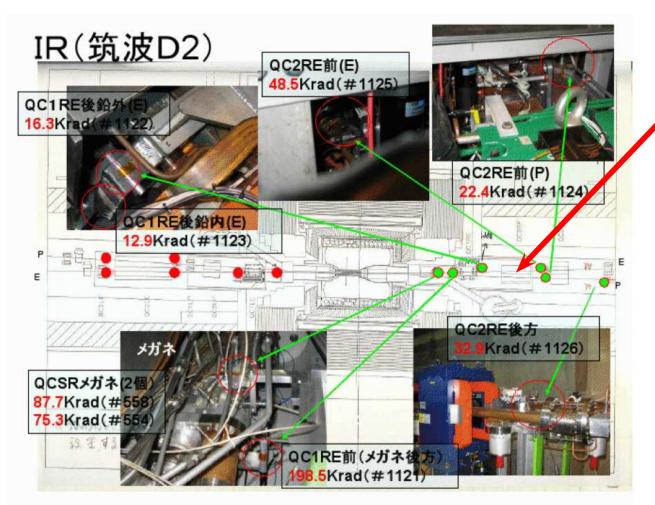




Radiation issues

- From DAQ point-of-view, we worry the frontend electronics inside the detector (CDC / BPID / EPID)
 - Measured by Belle and scaled to Belle II: only 0.6 krad / year
 - Neutron flux: $O(Hz)/cm^2$
 - Configuration flash (Xilinx XCF) & optical transceivers (Avago AFBR-57R6APZ) damaged by a irradiation test in the KEKB tunnel (may be too harsh environment, further radiation tests scheduled)
 - Difficult to access, takes a few weeks to replace
- JTAG-on-LVDS over a LAN cable
 - Readback CRC of Virtex5 for monitoring
 - Recovery from SEU by reprogramming, tested during the KEKB tunnel irradiation





Placed inside a lead box

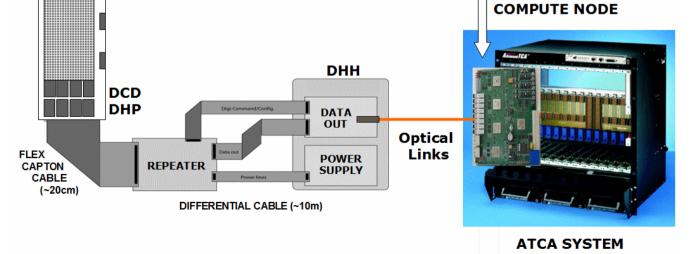


- Tested only for one device for last 2 months of KEKB
- 4.4 kRad per week (by TLD)
- 0.4 rad of thermal neutron
- 7.3 kHz/cm² high energy (>100 MeV) neutron measured by Au \rightarrow ¹⁸⁵Os production rate (not existing inside Belle II)

PXD readout

8 M channel × 1–2% occupancy (80-160k hits / trigger)

- ~10 charged tracks in an event, only regions-of-interest are needed
- Tracks reconstructed by a hardware SVD tracker and/or HLT system, RoI selected by ATCA system or PC with PCIe optical receiver
- RoI selection happens only after 5s of HLT processing time
 - 20μ s to readout the entire ladder
 - Multiple triggers may overlap in a single frame
 - *May conflict with SuperKEKB continuous injection scheme*



40 ladders, DCD-DHP-DHH chains to ATCA/PC

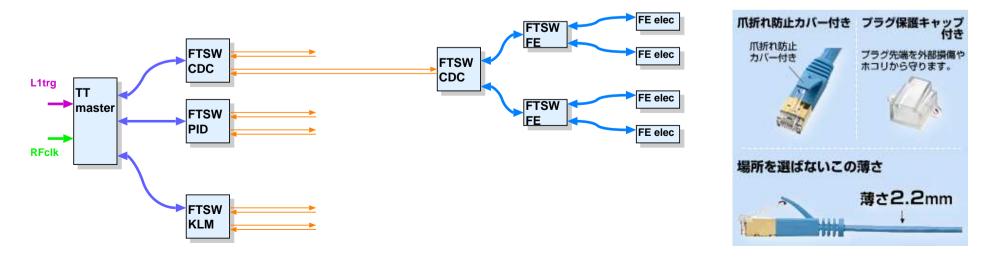
Readout summary

#ch	осс (%)	#link	/link (B/s)	#CPR	ch sz (B)	ev sz (B)	total (B/s)	/CPR (B/s)
PXD 8M (pixel detector)	1	40	182M	—	4	320k	7.2G (before R	ol)
SVD 243456 (silicon vertex detecto	1.9	80	6.9M	80	4	18.5k	555M	6.9M
CDC 15104 (central drift chamber) 10	300	0.6M	75	4	6k	175M	2.3M
BPID 8192 (barrel particle ID / tim	2.5 e-of-propo	128 agation)	7.5M	8	16	4k	120M	15M
EPID 77760 (endcap particle ID / d	1.3	138	0.87M	35	0.5	4k	120M	15M
ECL 8736 (Csl electromagnetic of	33	52	7.7M	26	4	12k	360M	15M
BKLM 21696 (glass-RPC barrel K_L/μ	1	86	9.7M	6	8	2K	60M	10M
EKLM 16800 (scintillator tile endcap	2	66	19.5M	5	4	1.4k	42M	8.4M

- 1.4GB/s total bandwidth without PXD
- \circ ~1000 optical links to readout the entire system
- Up to 300–400 COPPERs, rearrangeable according to the rate

Timing system

- L1 trigger & clock delivered to every front-end board
- Pipeline status is monitored to avoid buffer overflow signals collected from the frontend and COPPERs
- Deadtime only due to frontend buffer structure
- Entire system is synchronized to reduced RF clock (127 MHz) and beam revolution (100 kHz)
- Inter-connected by a thin CAT7 cable, or optical fibres between detector and electronics-hut



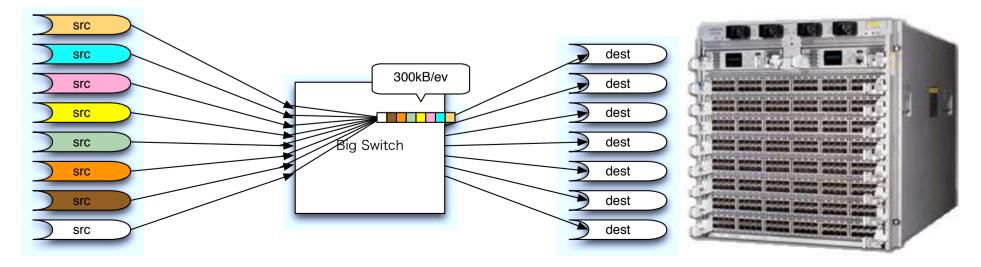
Timing system

- Entire system is synchronized to a reduced RF clock (127 MHz) and beam revolution (100 kHz)
- Trigger timing and status information embedded in a serialized signal (Xilinx OSERDES)
- 8b10b-encoded 32bit word at 254Mbps (every 157 ns)
- One type of PC board to cover all
 - 1-to-20 distribution using LVDS embedded in CAT7
 - 1-to-4 distribution using optical ports on FMC
 - ~1000 destinations in total



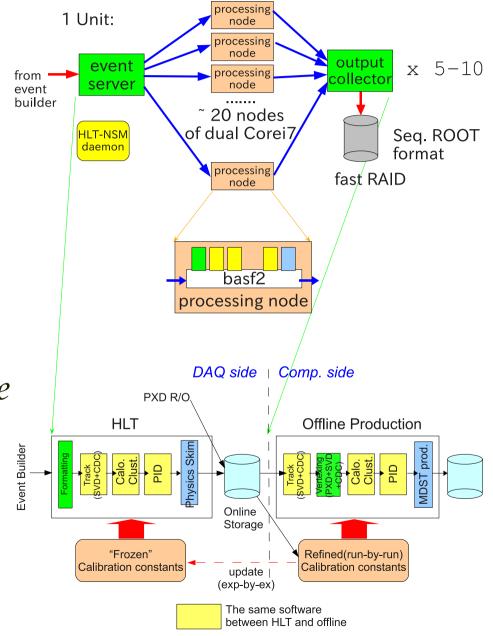
Event building

- \sim 50× GbE input, \sim 10× 10 GbE output, multi GB/s
- Large network switch (e.g. ARISTA 7500 series) (or cascading smaller switches as a backup option)
- Large enough buffer (>300kB buffer / port) to avoid data loss / retransmission
- IOGbE port tends to be expensive bundle multiple GbE into 10GbE by a smaller switch before feeding into the large switch



HLT

- The same offline software running online (basf2 framework)
- Frozen calibration constants are used faster updating is under consideration
- 5 sec latency to provide track information to PXD or save all hits if it takes more
- Physics skim to reject junk events (#track, #clulster, E_{ECL}, event topology, ...)



Summary

- Belle II construction has officially started, data acquisition system are on the track as well U
 - 8 subdetectors, 30 kHz L1 rate, multi-GB/s bandwidth

and will be ready in next 3 years

- Decision making and prototyping work on going, potential issues to be hopefully resolved soon
- Participation to Belle II is always highly welcome U
 shortage of electronics people in many places