Data Acquisition System for Belle II

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At the Belle II upgrade of the Belle experiment at KEKB, we expect about 20 kHz level-1 trigger rate at the design luminosity of 8 times 10ˆ34/cmˆ2/s. The Belle II data acquisition system is designed to read out the data from the entire detector at up to 30 kHz, with minimum amount of deadtime of several percent that is unavoidable due to hardware constraints. The system consists of subsystems for timing distribution, data links, event building and high level triggering. We present the system which is designed to be ready in 2013 for the start of Belle II.

Summary

At the Belle II upgrade of the Belle experiment at KEKB, we expect about 20 kHz level-1 trigger rate at the design luminosity of 8 times 10ˆ34 /cmˆ2/s. The Belle II consists of subdetectors for vertexing with pixels and silicon strips, tracking, particle identification, electromagnetic calorimetry, and muon detection. The Belle II data acquisition system is designed to read out the data from the entire detector at up to 30 kHz. The level-1 trigger is based on redundant tracking and calorimeter trigger, with both of them more than 99% efficiency is achieved for B meson decay events which gives 1 kHz rate, and physics triggers (light-quark-pair, tau-pair, QED and two-photons) that give another ˜10 kHz rate.

The system consists of subsystems for timing distribution, data links, event building and high level triggering. As was done in Belle, we aim for as much unification as possible in the individual steps in order to minimize especially the maintenance cost for the operation of 10 years. However, the pixel detector produces 10 times larger data than the rest of the system and requires a special handling.

The key for the unification is the data link (Belle2Link) which collects digitized data in the front-end electronics inside or near the detector, and transmits to a common pipeline platform for electronics readout (COPPER) modules where the data is formatted and sent out the event building system. Belle2Link is implemented over the Xilinx RocketIO high speed serial link technology. The number of links is a few hundred per subdetector.

We minimize the deadtime fraction to several percent which is unavoidable due to hardware constraints. The timing distribution system distributes a system-wide clock that is synchronized to the accelerator, the trigger signal, and related information over a slower serial link. Up to five triggers are processed in a pipeline with about 30 micro second latency. The responses are also collected in a pipeline.

The data bandwidth is dominated by the pixel data, which produces up to 24 GB/s of data after zero suppression. We reduce this by a factor of 10 using a two-step track matching procedure: first, tracks are calculated inside an ATCA system of inter-connected FPGA-based computing nodes from four layers of silicon strip detector information and matching pixels are saved, and then track information from high level trigger system after five seconds is used to save more pixels. Therefore, event building is done in two steps, for everything other than pixel, and high level trigger output and pixel.

The system is designed to be ready in 2013 for the start of Belle II.

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