universitätbonn

SI LAB
Silizium Labor Bonn

A serial powering scheme for the ATLAS pixel detector at sLHC

L. Gonella, D. Arutinov, A. Eyring, M. Barbero, F. Hügging, M. Karagounis, H. Krüger, N. Wermes

TWEPP 2010, Aachen, 21/09/2010

Outlook

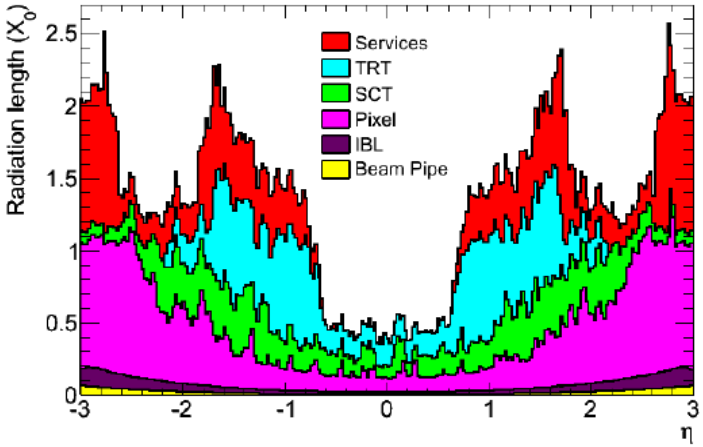
- ATLAS pixels powering needs
- Serial powering
- Serial powering scheme for ATLAS pixels @ sLHC
  - Scheme architecture
    - Shunt-LDO
    - AC-coupling
    - Stave protection
  - Prototyping status
  - Material budget calculations
- Conclusions

ATLAS pixels powering

LHC → sLHC			
FE channels:	~80M	→	~455M
Total FE power:	6.7kW	→	12.3kW
Total FE current:	3.8kA	→	6kA

→ x5-6 granularity
→ x2 power
x3 current

- @LHC: independent powering
  - 20% efficiency
  - Very massive services
    - High x/X0%, saturated cable channels
- @sLHC
  - Independent powering is unfeasible!
  - Need to transmit power at low currents → lower V_{drop}
    - Higher power efficiency
    - Reduced cables cross section

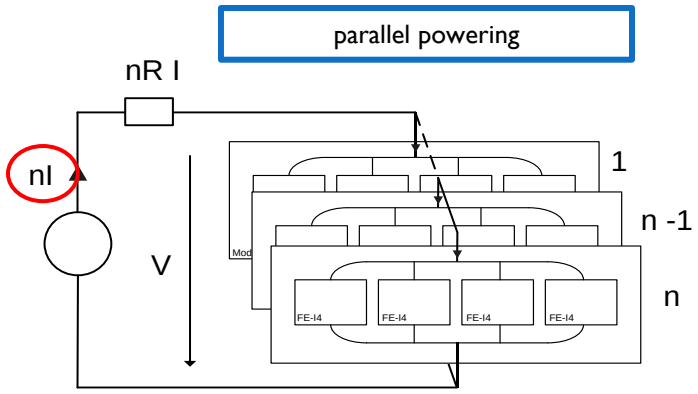


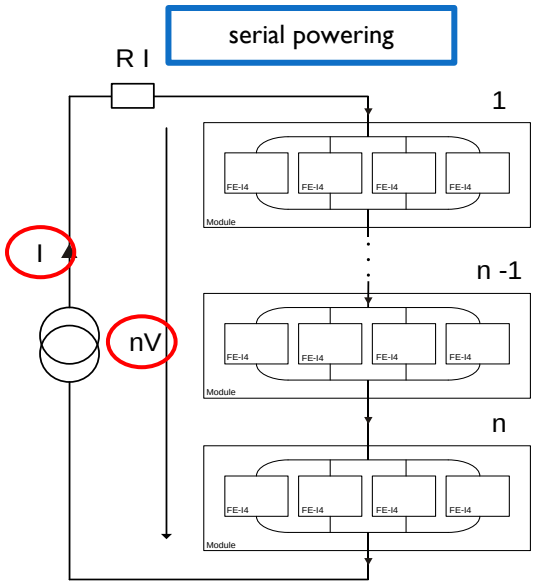
ATLAS inner det. material distribution (incl. IBL)

→ Serial powering or DC-DC conversion

Serial powering

- Allows transmitting power at low currents and high voltages
  - A chain of n modules is powered in series by a constant current I
  - Current to voltage conversion is performed locally (on chip/module) by regulators
- Key facts
  - I scales of a factor n, with respect to parallel powering
  - V_{drop} is limited only by the power density and the I source output voltage capability
    - Allows optimal trade off between efficiency and material





Regulators: on or off chip?

Ratio of converter/detector Figure Of Merits (FOM) → radiation thickness penalty for using converters in active areas

- FOM for silicon detectors: (load resistance) x (active area)
  - Pixels = 10 $\Omega \cdot cm^2$
  - Strips = 100 $\Omega \cdot cm^2$
- FOM for converters: $\varepsilon/(1-\varepsilon)$ x (output resistance) x (x/X0) x (area)
  - External converters =1-5% x/X0 $\cdot \Omega \cdot cm^2$ @ 80% efficiency

→ Penalty for pixels = 0.5% x/X0 per layer
→ Penalty for strips = 0.05% x/X0 per layer

- Penalty >0.2% x/X0 per layer too severe
  - Target for ATLAS pixels @ sLHC < 2% x/X0 per layer

→ Strips can use external converters
→ Pixels must use internal/on chip converters

On-chip regulators for SP

- FE needs analog and digital voltage → 2 regulators/FE
- Redundancy → Connect all regulators on module that take I_{in} in parallel
  - In case of failure of one regulator, the current can still flow through the other regulators on the module and the power chain is not interrupted

REGULATOR REQUIREMENTS

Very robust against mismatch and process variation
Able to cope with increased input current

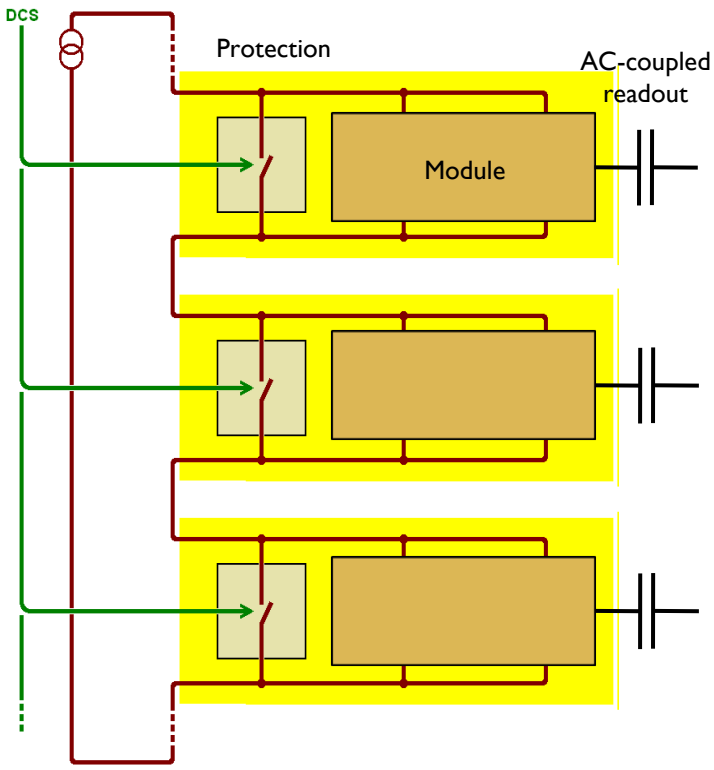
System aspects

AC-coupled module readout

- Modules in a chain are on different gnd

Stave protection

- Assure supply of power to the SP chain in case of failures
- Allow power to arbitrary selection of modules
- Requirements
  - Slow Control
  - Fast Response
  - Low power density
  - Minimal x/X0
  - Radiation hardness

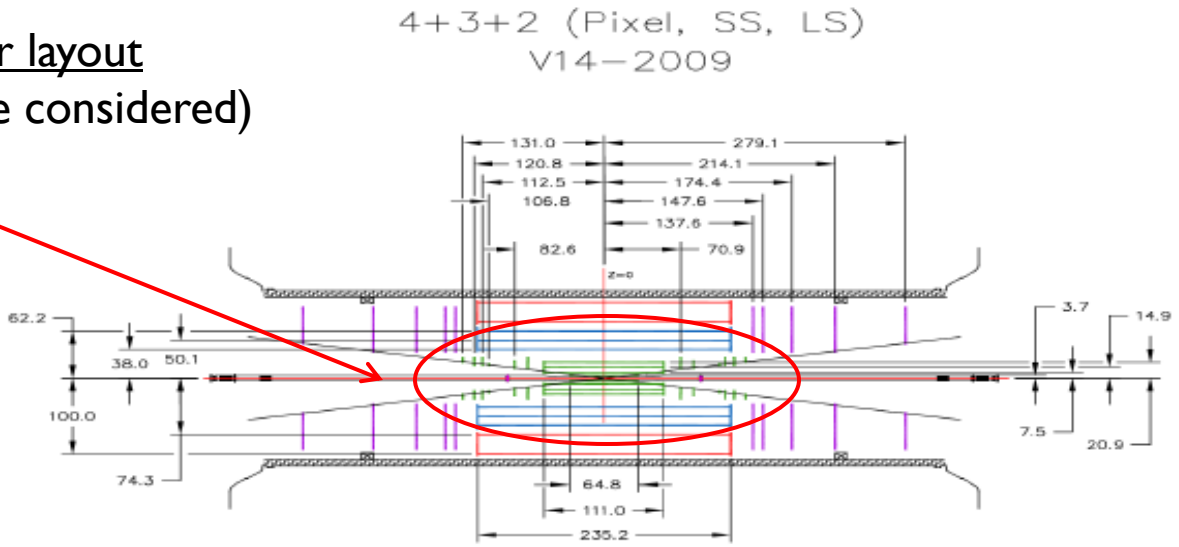


SP for ATLAS pixels @sLHC

Current pixel detector layout

4 barrel layers (5th one considered)

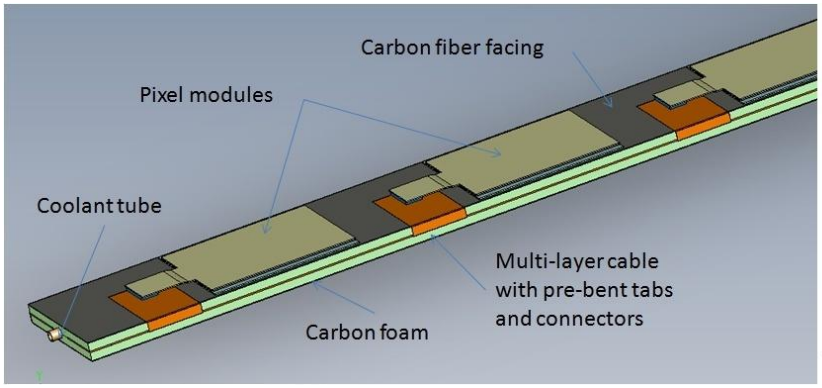
5 disks/side



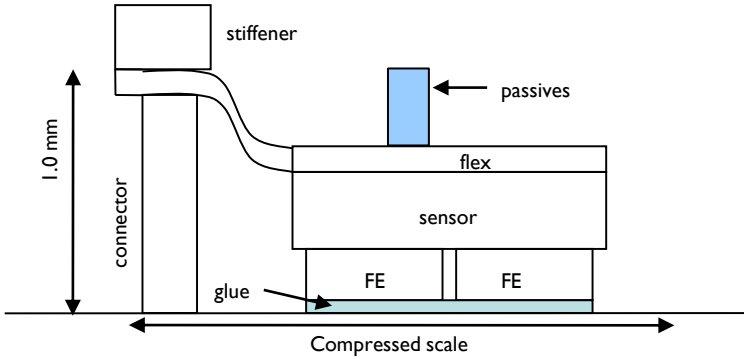
- Starting point for development of a SP scheme: pixel outer layers
  - Technology to build them is available
    - Planar sensors on 6” wafer
    - FE-I4 with minor differences wrt. IBL
    - GBT system for data
  - A stave concept is being developed
  - Entering the prototyping phase

sLHC outer layers

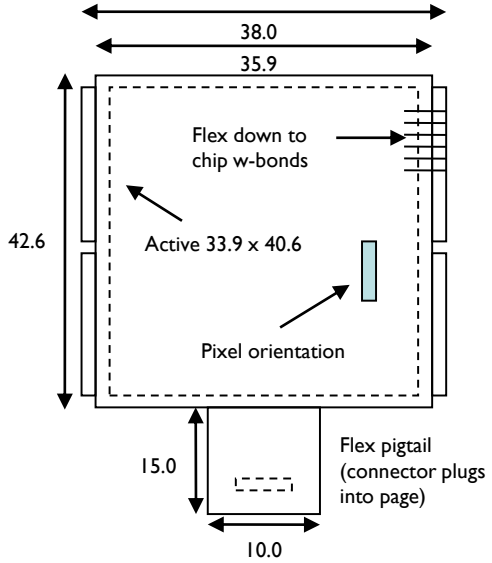
- 32 modules/stave
  - 16 top, 16 bottom
  - 2x2 FE-I4 modules
- Electrical unit = ¼ stave (i.e. 8 modules)
  - 1 stave cable/el. unit
  - 1 EOS card/el. unit



Module side view

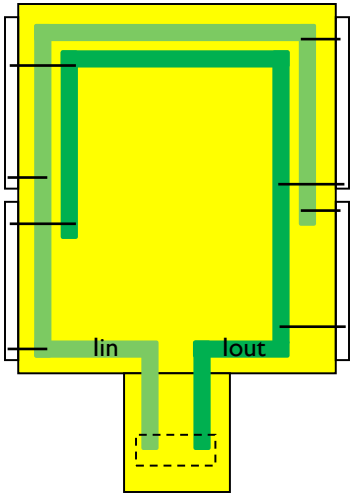


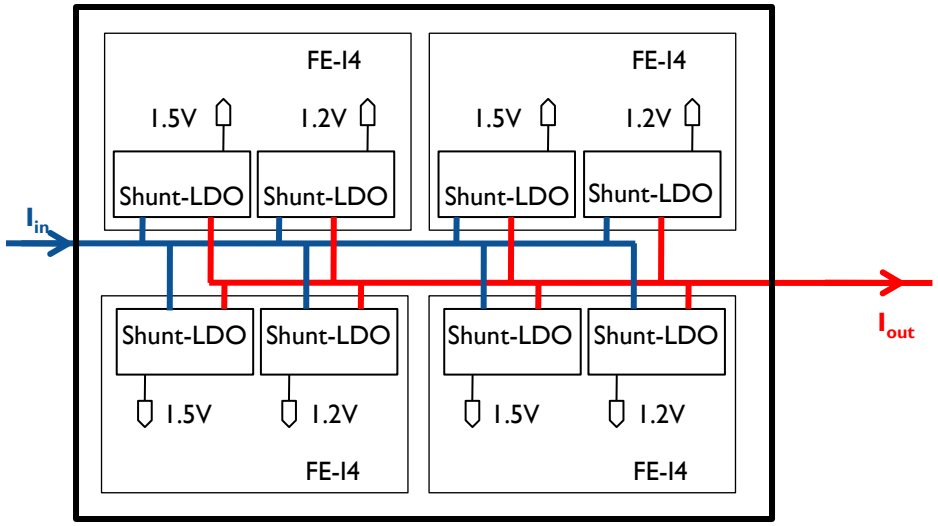
Module top view



Current (i.e. power) to the modules

- Current delivered to the modules via stave cable and module flex
  - Power unit = electrical unit = 8 modules
  - $I_{tot} = I_{mod} = \sim 2.4\,A$
    - FE-I4 nominal current = ~600 mA
- Current to voltage conversion on-chip → Shunt-LDO
  - 2 Shunt-LDO/FE to generate VDDA = 1.5 V and VDDD = 1.2 V
  - 8 Shunt-LDO on the module operate in parallel

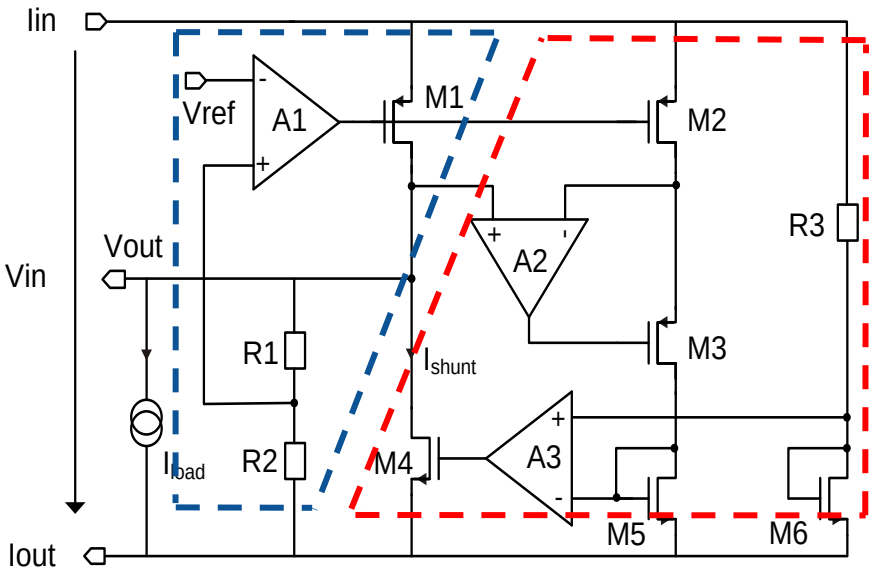




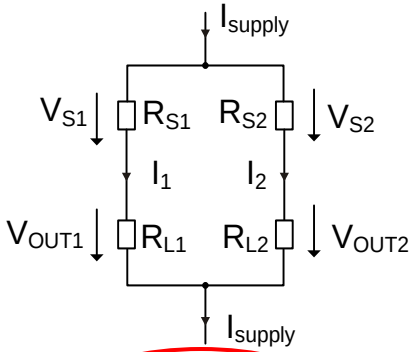
Shunt-LDO working principle

Combination of an LDO and a shunt transistor

Shunt-LDO: simplified schematic



2 Shunt-LDOs in parallel: equivalent circuit



→ Shunt-LDO can be placed in parallel without problems due to mismatch
→ Shunt-LDO with different V_{out} can be placed in parallel
→ Shunt-LDO can cope with increased I_{in}
→ Normal LDO operation when shunt circuitry is off

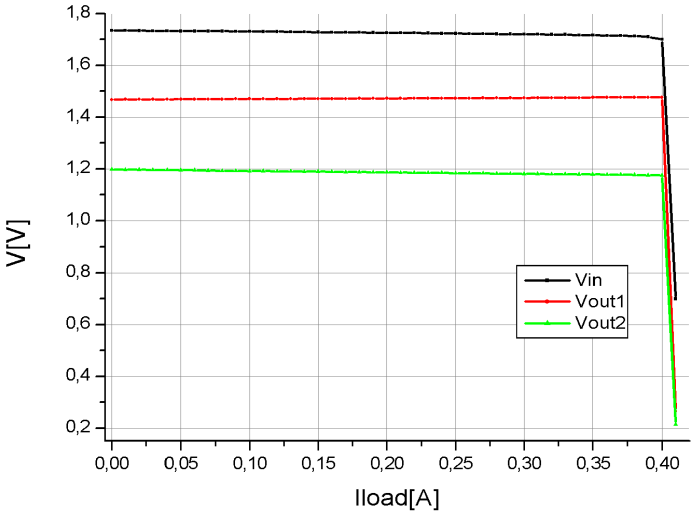
Shunt-LDO characterization

Working principle and good performance demonstrated by 2 prototypes

2 Shunt-LDO in parallel generating different V_{out}

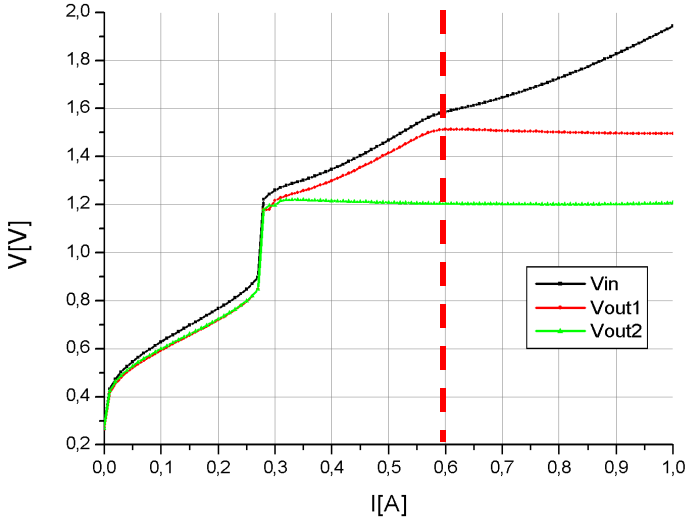
Load regulation

- V_{in} and V_{out} stable until (I_{load1} + I_{load2}) = I_{supply} (= 0.8 A)
- Effective R_{out} = 60 mΩ (incl. wire bonds and PCB traces)



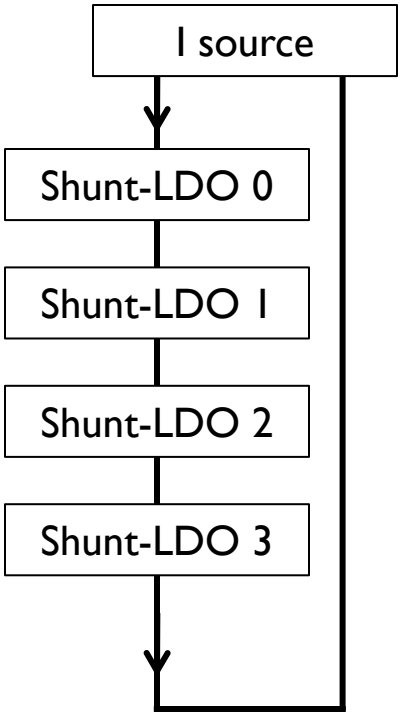
V_{out} generation

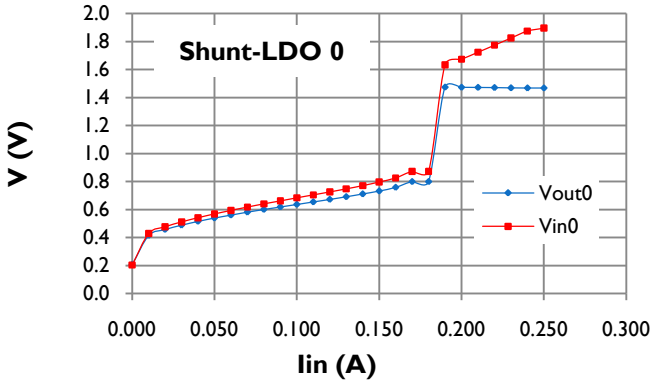
- After saturation
  - V_{out} settle @ different potentials
  - R_{in} ≈ 2 Ω

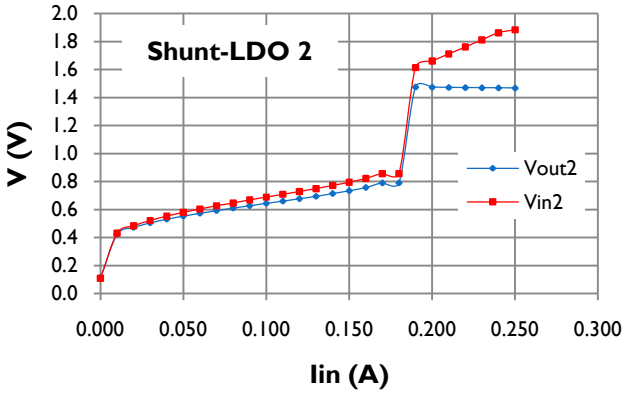


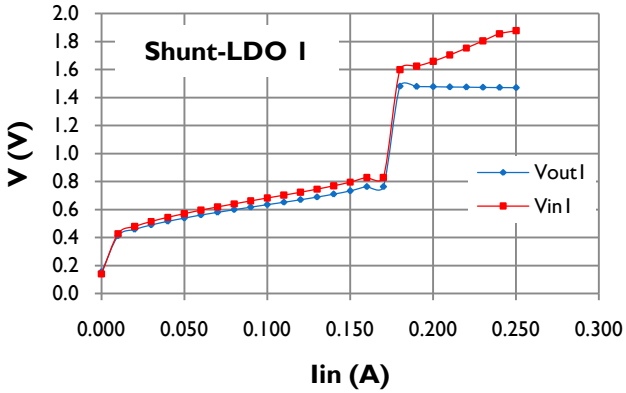
Shunt-LDO in a serial powering chain

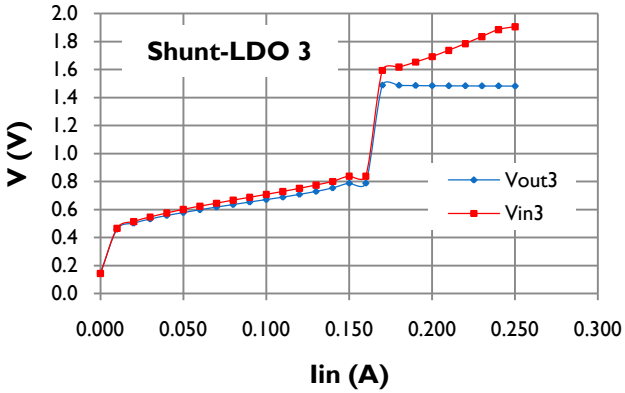
4 Shunt-LDOs in series generating V_{out} = 1.5V







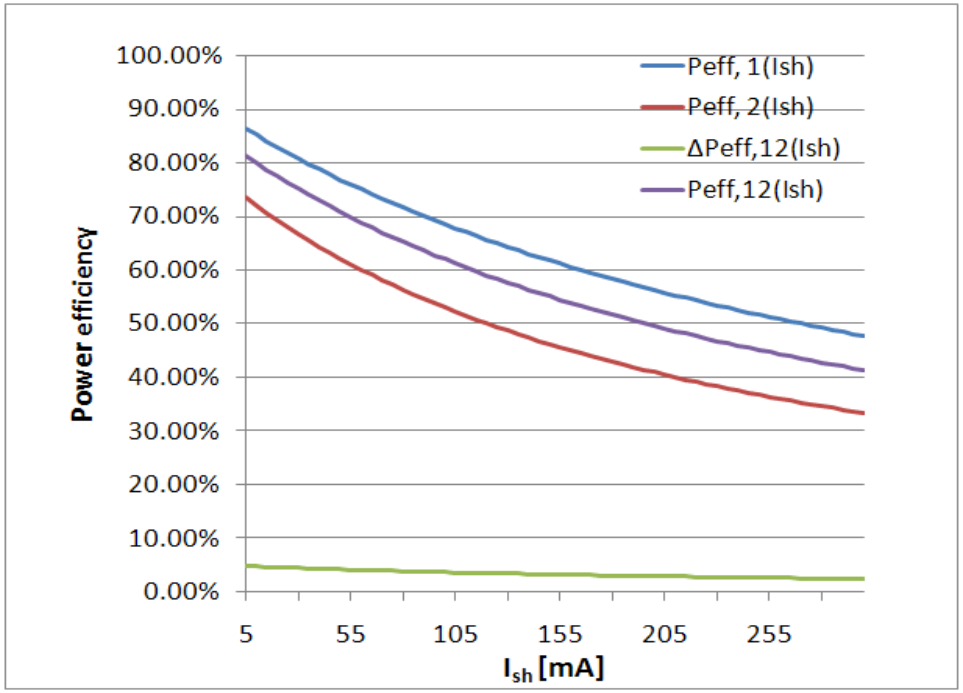




Shunt-LDO efficiency

- Shunt-LDO sources of inefficiency
  - LDO dropout voltage V_{drop}
  - I_{shunt}
  - ΔV between the 2 V_{out} needed by the FE
- Calculation for ATLAS Pixels

	nominal	worst case	best
V_{out1} [V]	1.4	1.4	1.4
V_{out2} [V]	1.2	1.2	1.2
I_{out1} [A]	0.36	0.4	0.36
I_{out2} [A]	0.24	0.27	0.24
V_{drop} [V]	0.2	0.2	0.1
I_{shunt}[A]	0.03	0.05	0.01
ΔU [V]	0.2	0.3	0.2
I_{TOT} [A]	0.6	0.67	0.6
P_eff, 1	80.77%	77.78%	90.81%
P_eff, 2	66.67%	59.56%	76.80%
P_eff, 1-2	79.55%	76.14%	90.32%
ΔP_eff,1-2	4.55%	6.57%	5.16%
P_eff,1-2g	75.00%	69.56%	85.16%

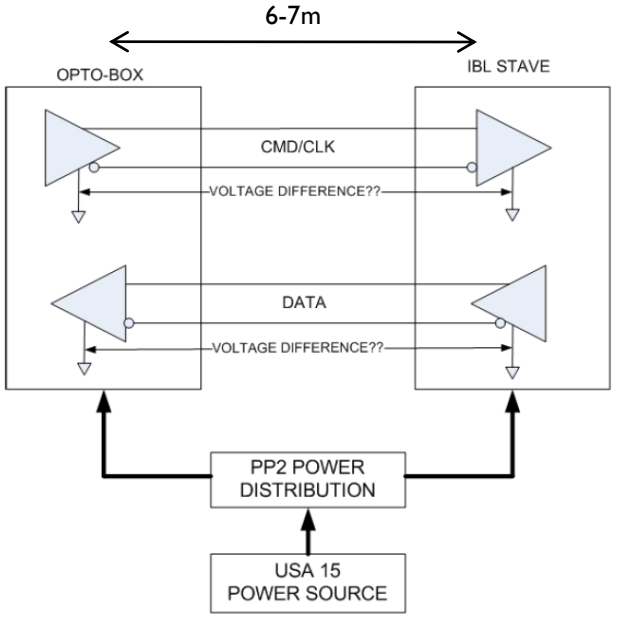


AC-coupling

Widely used termination technique in telecommunications

- Optimal V_{CM} at RX input
- Level shifting
- Guard against differences in ground potential

- Needed for module readout in a serial powering scheme
- Independently of the powering scheme might be needed for the ATLAS pixels upgrade
  - @IBL
    - Concerns about long data transmission lines
    - Discussion already started about possible need for AC-coupling
  - @sLHC
    - Possible compatibility issues between FE-I4 and GBT standards → LVDS vs. JESD8-13: SLVS-400



Possible AC-coupling implementations

Favorite option: direct AC-coupling at RX input

Simple, low material

Requires self biased RX input & DC-balanced data

Downlink: clk & cmd

- FE-I4 RX input self biased
- clk inherently DC-balanced
- cmd are not DC balanced but
  - Slow data (40MHz)
  - Rail-to-rail receiver, i.e. can accommodate some V_{CM} shift arising from non-DC balanced data

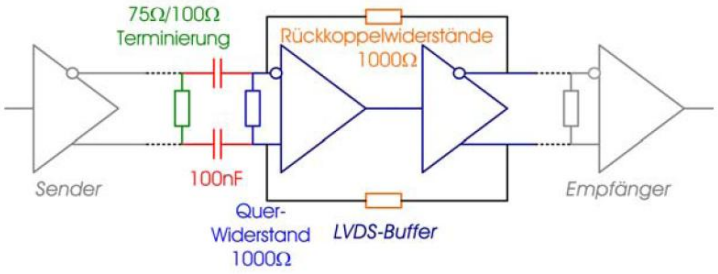
Uplink: data

- FE-I4 data are 8b10b encoded
- GBT accepts any encoding
  - RX inputs do not have integrated self biasing circuitry, but this could eventually be done externally

Alternative option: link with feedback

Successfully used for the SP proof of principle

Higher complexity, more material



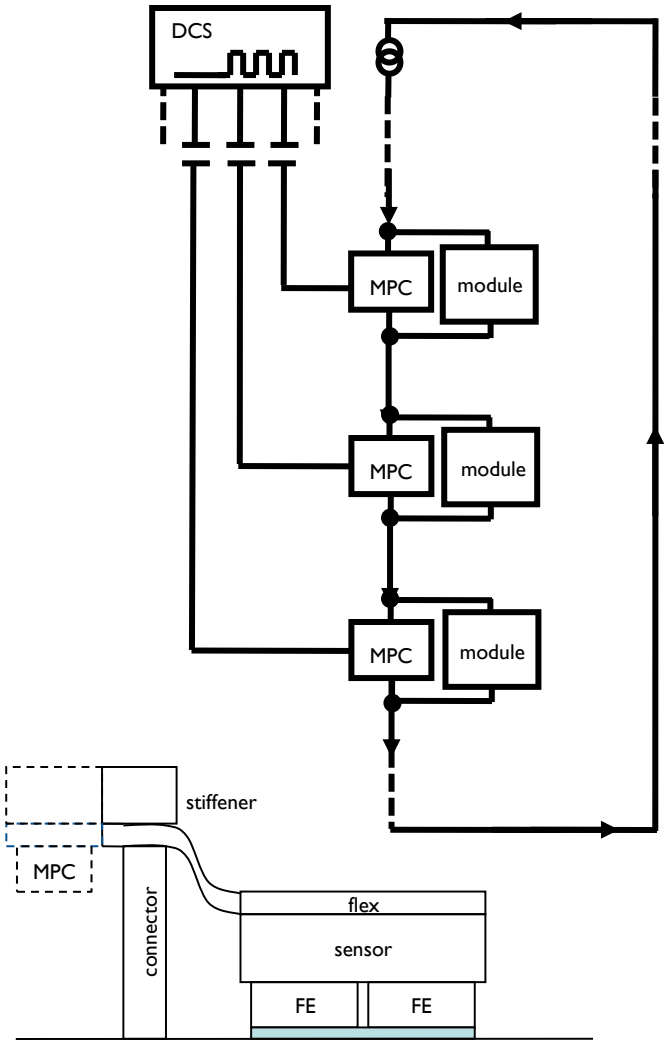
Stave protection

Proposed protection scheme

- 1 Module Protection Chip/module
  - Could be placed on pigtail
- 1 AC-coupled slow ctrl line/MPC from the DCS
  - 8 lines/stave cables
  - One capacitor/line on the DCS side

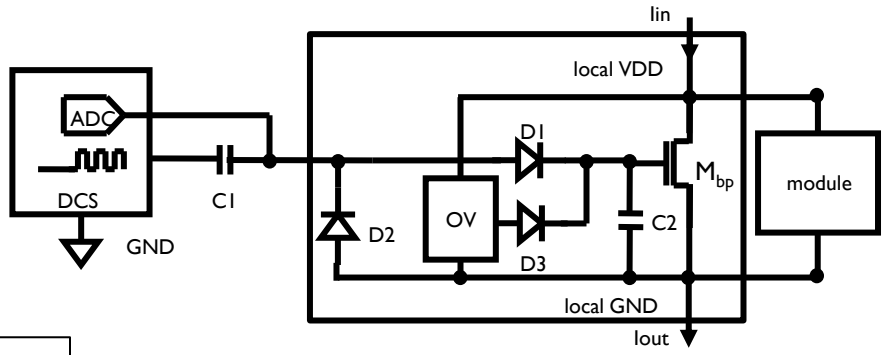
Working principle

- DCS can switch on/off selected modules via slow ctrl line
- In case of overvoltage
  - Fast response circuitry in MPC reacts
  - DCS switches off the module
- MPC can be used also for power on sequence

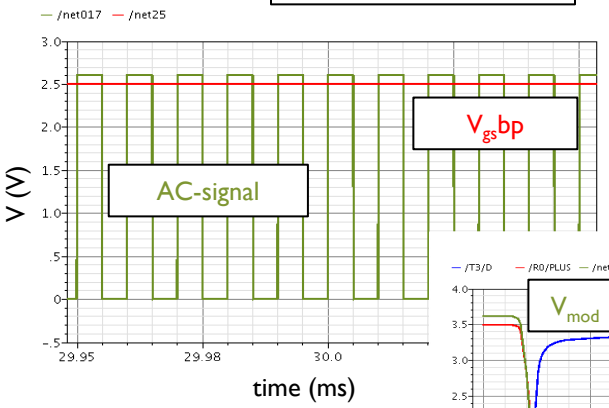


Module protection chip

- 130nm IBM
- Bypass transistor
- Independent slow ctrl line & OV protection
  - OV protection = Silicon controlled rectifier
- Preliminary simulations:

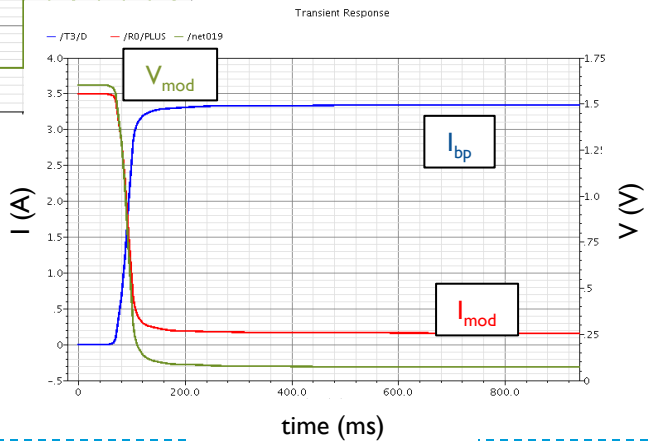


Slow ctrl



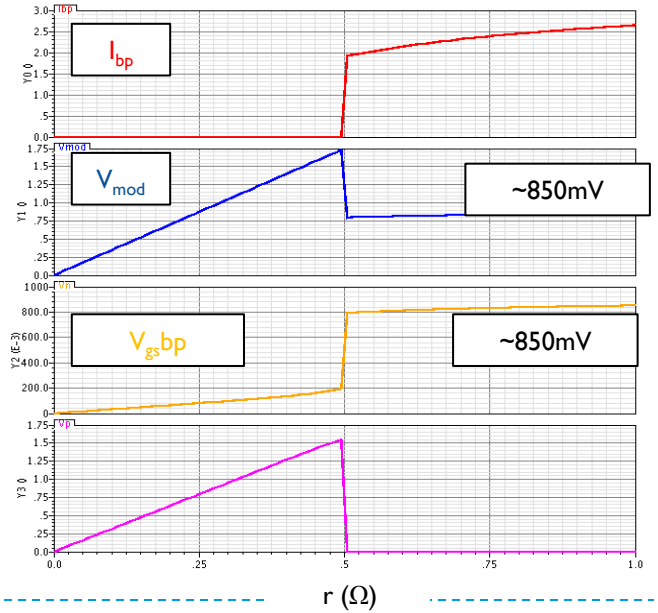
Bypass

DGNMOS
W = 48mm
L = 0.24µm



C1 = 100nf
C2 = Cgs = 33pf
D1, D2 = PMOS

Fast response

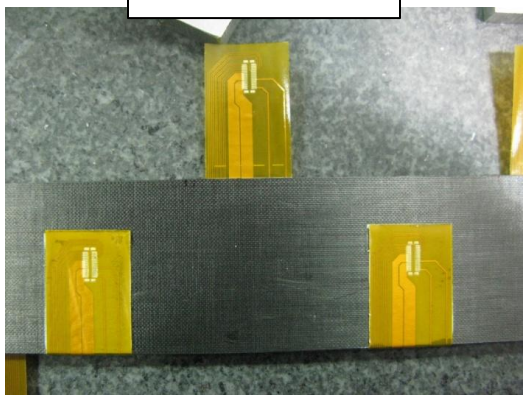


Prototyping

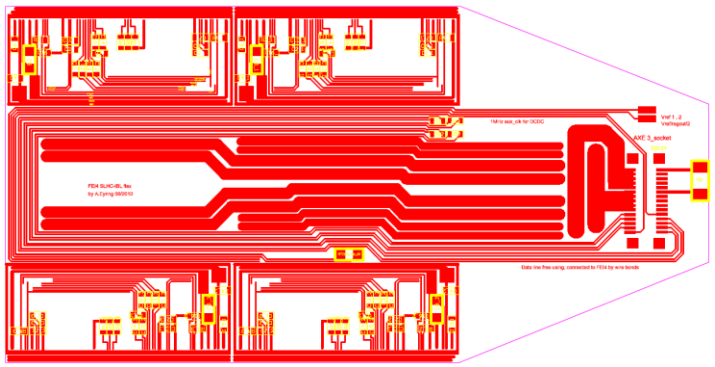
Goal: prototyping an sLHC pixels outer layer with serial powering to try the concept extensively

- Outer pixel layers prototyping started in the pixel collaboration
  - 4-chip sensor design in production, FE-I4 submitted
  - stave cable and type1 cables already prototyped
  - In progress: stave mechanics and cooling studies, EOS cards design, …
- Serial powering related activities in Bonn
  - Design of LV lines on stave cables
  - Design of module flex: 1st prototype in production
    - Allows testing SP, direct powering, direct powering with DC-DC

Stave cable



Module flex



x/X0: SP vs. DC-DC – active area

Direct powering with DC-DC conv → fixed V_{drop} between V source and converter

@sLHC: voltage regulator on PP1, x2 charge pump DC-DC converter in FE-I4

→ 0.2V on stave, 0.8V on Type I services

x/X0% LV lines (Al only)

DC-DC conv: Vdrop = 0.2V

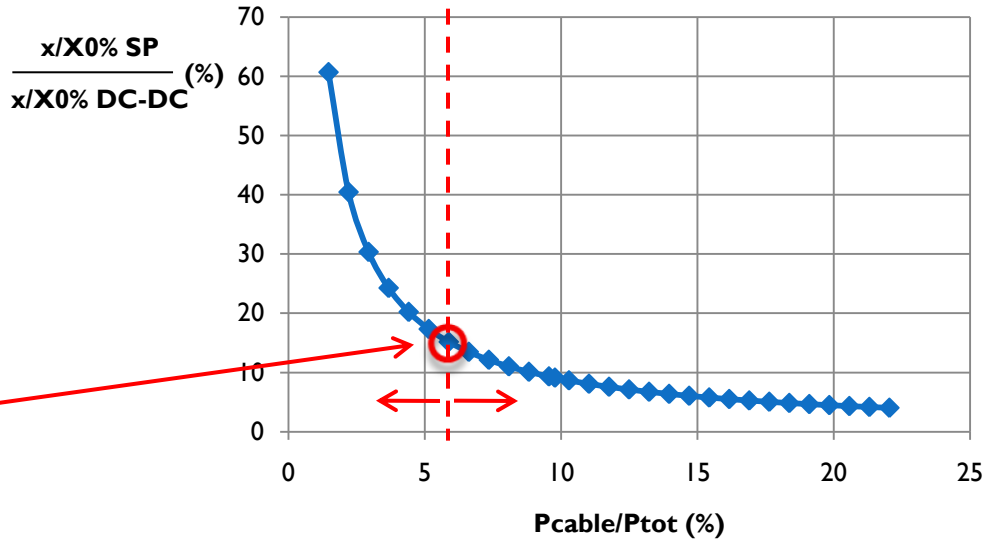
→ P_{cable} = 5.56% P_{tot}

→ LV cables: 0.093% x/X0

SP @ P_{cable} = 5.88% P_{tot}

→ LV cables = 0.014% x/X0

→ ~85% less material



Serial powering

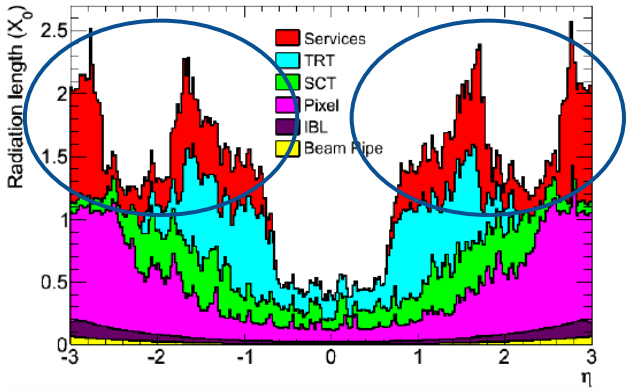
LV lines (Al + kapton) :	0.056% x/X0
AC-coupling C:	0.018% x/X0
Protection:	0.010% x/X0
Total:	**0.084% x/X0**

Direct powering w/ DC-DC conversion

LV cable (Al + kapton):	0.139% x/X0
External C:	0.015% x/X0
Total:	**0.154% x/X0**

x/X0: SP vs. DC-DC – large η

- Services dominate the material budget
- Cable channels are saturated



ATLAS inner det. material distribution (incl. IBL)

DC-DC conv: V_{drop} = 0.8V → LV cables: 2827.2mm^2 Al x-section
SP @ V_{drop} = 0.8V → LV cables: 684mm^2 Al x-section

x/X0 SP ≤ **0.25** x/X0 DC-DC

Conclusions

A serial powering scheme for the ATLAS pixel detector at sLHC is being developed at Bonn University

- Scheme architecture definition, power efficiency and material budget calculations ongoing
- A custom developed new regulator concept targeting serial powering has been developed: Shunt-LDO
  - 2 prototypes confirmed working principle and good performance
  - 2 Shunt-LDOs/FE-I4
- AC-coupling and protection schemes have been proposed
  - FE-I4 LVDS RX designed with self-biased inputs for direct AC-coupling with DC-balanced data
  - Simulation of a Module Protection Chip started
- Prototyping of an ATLAS pixel detector outer layer featuring serial powering for sLHC has started