

A serial powering scheme for the ATLAS pixel detector at SLHC

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Powering of future trackers at SLHC requires low current distribution for high power efficiency and low material budget. In this framework, we investigate a serial powering scheme for the ATLAS pixel detector at SLHC. A dedicated regulator has been prototyped and largely characterized, both as single device and in a serial powering configuration. System aspects, such as AC-coupled module readout, are investigated with a pixel stave emulator, and the effort is now converging to the development of a serially powered outer layer stave prototype. Results and status of each activity will be presented.

Summary

The parallel powering scheme used for current LHC trackers suffers of low efficiency and is very massive. In the present ATLAS pixel detector for instance, power efficiency is of only 20%, services dominate the material budget, and cable channels are saturated. At the higher currents needed for the SLHC trackers, this powering scheme will fail. To reach high power efficiency while keeping the material budget low in future trackers, power should be transmitted at low current. To this aim, a serial powering scheme is being developed for the ATLAS pixel detector at SLHC. In serial powering, a constant current source provides current to a series of n modules, thereby reducing the voltage drop on the cables by a factor $1/n$ with respect to parallel powering. The most important gain however will be in terms of material budget. This powering scheme in fact allows a significant reduction of the number of cables needed and of their copper cross section. Regulators installed locally, i.e. on module or on chip, generate the analog and digital voltages needed for FE operation. In the case of pixel detectors, the regulator has to be on chip, as the penalty in terms of material budget for using external converters would be too high. The new ATLAS pixel detector front-end FE-I4 integrates 2 Shunt-LDOs. This new regulator concept is a combination of a Low Drop Out (LDO) voltage regulator and a shunt regulator, designed to match serial powering requirements. Its robustness against process variation and mismatch allows safe parallel operation of all the Shunt-LDOs on a module, which adds redundancy to the scheme. Moreover, Shunt-LDO can cope with increased current should one of the parallelly placed regulators fail. Two prototype iterations demonstrate working principle and good performance. Single device characterization and power efficiency will be presented. The performance of Shunt-LDOs in a serial powering configuration is studied as well. To this purpose, a serially powered pixel stave emulator has been set up using the latest Shunt-LDO prototype. Results are good and in agreement with single device characterization. This test bench allows also investigation of an AC-coupling scheme for readout of modules in a serial powering chain, using the FE-I4 LVDS transmitter and receiver prototype chip. The proposed AC-coupling configuration will be discussed together with system aspects related to serial powering. Finally, as the outer layers of the ATLAS pixel detector at SLHC are entering a prototyping phase, our effort in the development of a serial powering scheme is focusing on this framework. On a conceptual level, the details of the scheme are being worked on, from the modules up to the current supply, including material budget and power efficiency calculations. As for the prototyping, we are starting to prepare the stave cable for serial power current routing, as well as designing a dedicated module flex. An overview of the serial powering scheme for the outer layers of the ATLAS pixel detector at SLHC will be given, and the status of the prototyping activities will be reported.

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