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Digital part of PARISROC2: a photomultiplier array readout chip

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PARISROC is the front-end ASIC designed to read 16 photomultiplier (PM) tubes for neutrino experiments. It' s able to shape, discriminate, convert and readout data in an autonomous and channel-independent mode. The tests made on PARISROC1 have shown some limitations on time measurements and on hit rate capability. In order to correct these points, the digital part of PARISROC2 has been completely modified to add new features and improvements. First, it integrates a new time to amplitude converter with less than 1 ns resolution. Secondly, conversion and readout has been speed-up by a factor of 4 to handle the PM hit rate. The chip was received in February 2010 and is now under test.

Summary

PARISROC (Photomultiplier ARray Integrated in Sige ReadOut Chip) is the front end ASIC designed for the PMM2 R&D project dedicated to neutrino experiments. Next generation of neutrino experiments that will take place in megaton size water tanks will require very large surface of photodetection and volume of data. For the project, this large surface of photodetection is segmented in macro pixels made of 16 Photomultiplier Tubes (PMT) connected to an autonomous front end ASIC: PARISROC.

The first release of this chip was received in October 2008 and fully characterised. It has shown some limitations which have been corrected in a second release submitted at the end of 2009.

It has been proven in simulation that to reduce the loss rate down to 0.3%, the trigger's treatment in PARISROC2 should be speed-up by a factor of 4. As conversion and readout take about 99% of the total cycle length, it has been decided to improve these 2 processes.

First, for the conversion, it has been demonstrated that the fine time resolution can be achieved with a 10-bit ADC. But, for the charge, 2 gains have been added in the analog part to fulfill the dynamic range (0-300 pe) with this reduced number of bits. So, the ADC is now counting 8, 9 or 10 bits: this allows us to divide by 4 the time for the analog to digital conversion compared to PARISROC1.

Secondly, the readout frequency has been increased to 40 MHz (multiplied by 4) and the number of bits in the readout frame has been slightly decreased thanks to a lower number of bits in the conversion. The readout frame, given below, is composed of 51 bits for each channel:

- Channel number: 4 bits
- Coarse time counter: 24 bits
- Extra coarse time counter: 1 bit
- Gain used: 1 bit
- Fine time: 10 bits
- Ramp used: 1 bit
- Charge: 10 bits

Moreover, for this new release, we also have integrated a completely new timing module which includes a new fine time and a new coarse time measurement. This will allow us to tag events with an increased accuracy (less than 1ns) and to remove the blind zones seen on the measurements of PARISROC1.

First, for the fine time, we have chosen to have 2 independent ramps with an overlap between them. These 2 ramps will be sampled at the same time and an internal module will tag the valid one. Finally, the digital part will convert and readout the selected ramp.

In Addition, the coarse time counter is now enhanced: it is able to detect triggers synchronous to the clock: this is done by using an extra 1-bit counter counting at the opposite edge of the clock. This counter is redundant with the least significant bit of the coarse counter and allows us to correct it offline.

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