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# Associative Memory design for the Fast TracK processor (FTK) at Atlas

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We describe a VLSI processor for pattern recognition based on Content Addressable Memory (CAM) architecture, optimized for on-line track finding in high-energy physics experiments. A large CAM bank stores all trajectories of interest and extracts the ones compatible with a given event. This task is naturally parallelized by a CAM architecture able to output identified trajectories, recognized among a huge amount of possible combinations, in just a few 100 MHz clock cycles. We have developed this device (called the AMchip03 processor), using 180 nm technology, for the Silicon Vertex Trigger (SVT) upgrade at CDF using a standard-cell VLSI design methodology.
We propose now a new design (90 nm technology) where we introduce a full custom standard cell. This is a customized design that allows to maximize the pattern density and to minimize the power consumption.
We discuss also possible future extensions based on 3-D technology. This processor has a flexible and easily configurable structure that makes it suitable for applications also in other experimental environments.

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