A Front End ASIC for the read out of the PMT in the KM3NeT Detector

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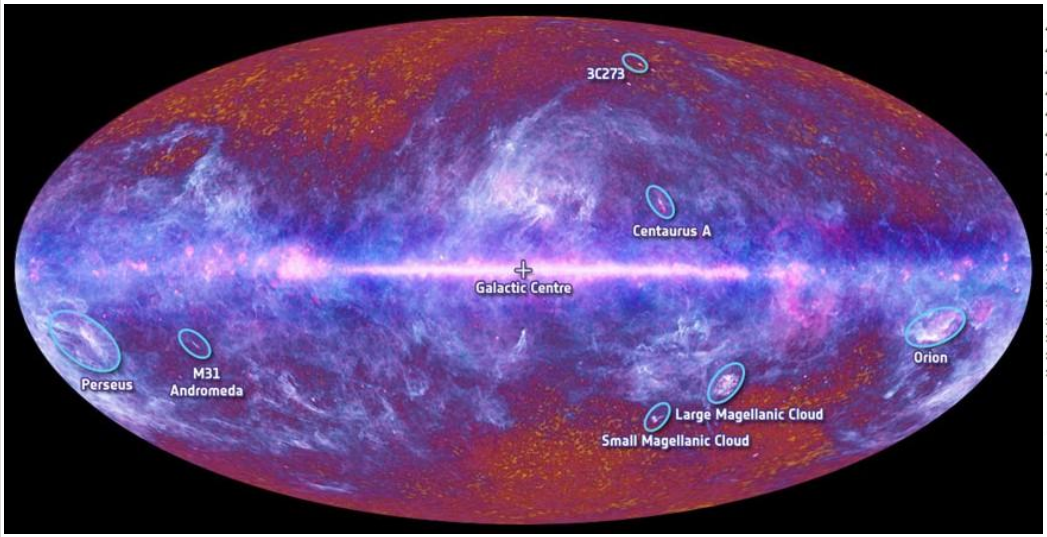
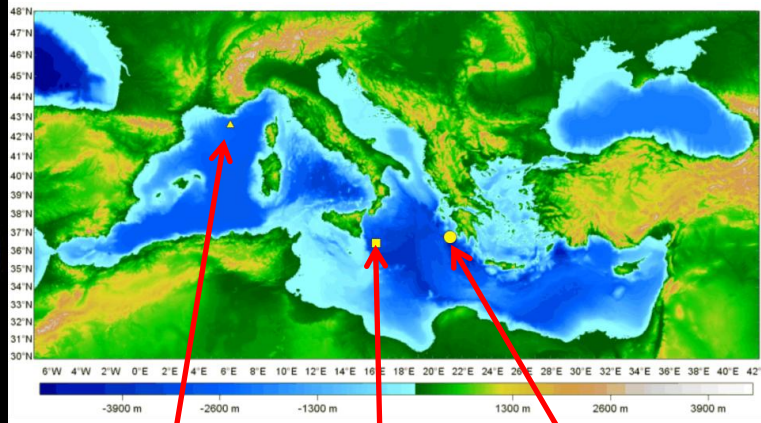
Contents

- Introduction to the KM3NeT Experiment.
- KM3NeT Detector Concept.
- Read out electronics.
- Specifications of the ASIC.
- The Circuit.
- Test Results.
- Conclusions & Future.

KM3NeT Experiment

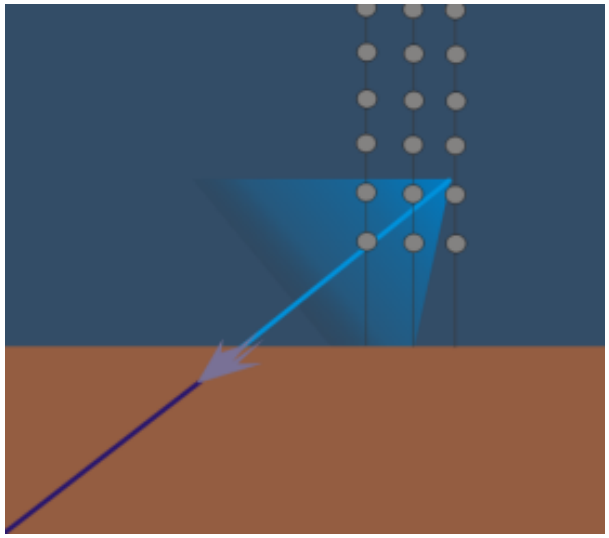
- Neutrinos are unique messengers from the most violent, highest-energy processes in our Galaxy and far beyond.
- Neutrino astronomy is experimentally highly demanding, requiring vast volumes of target material, such as water or ice & dark environment.

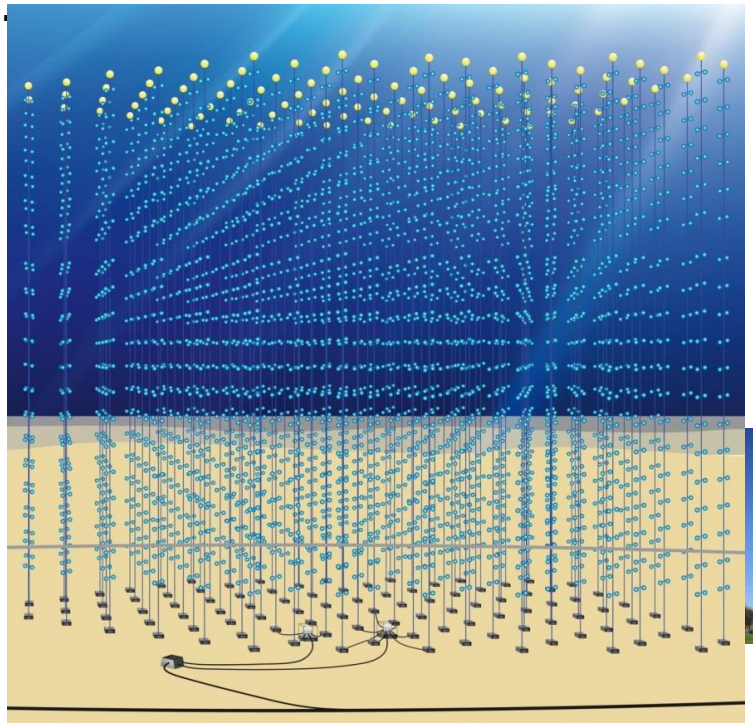




KM3NeT Detector concept

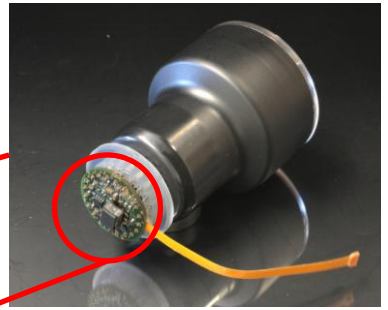
- The detection of high-energy muon neutrinos exploits the emission of Cherenkov light by the muon and other charged secondary particles produced in a neutrino interaction.
- Photo-Multiplier-Tubes (PMTs) housed in glass spheres (optical modules), are deployed in the deep sea.

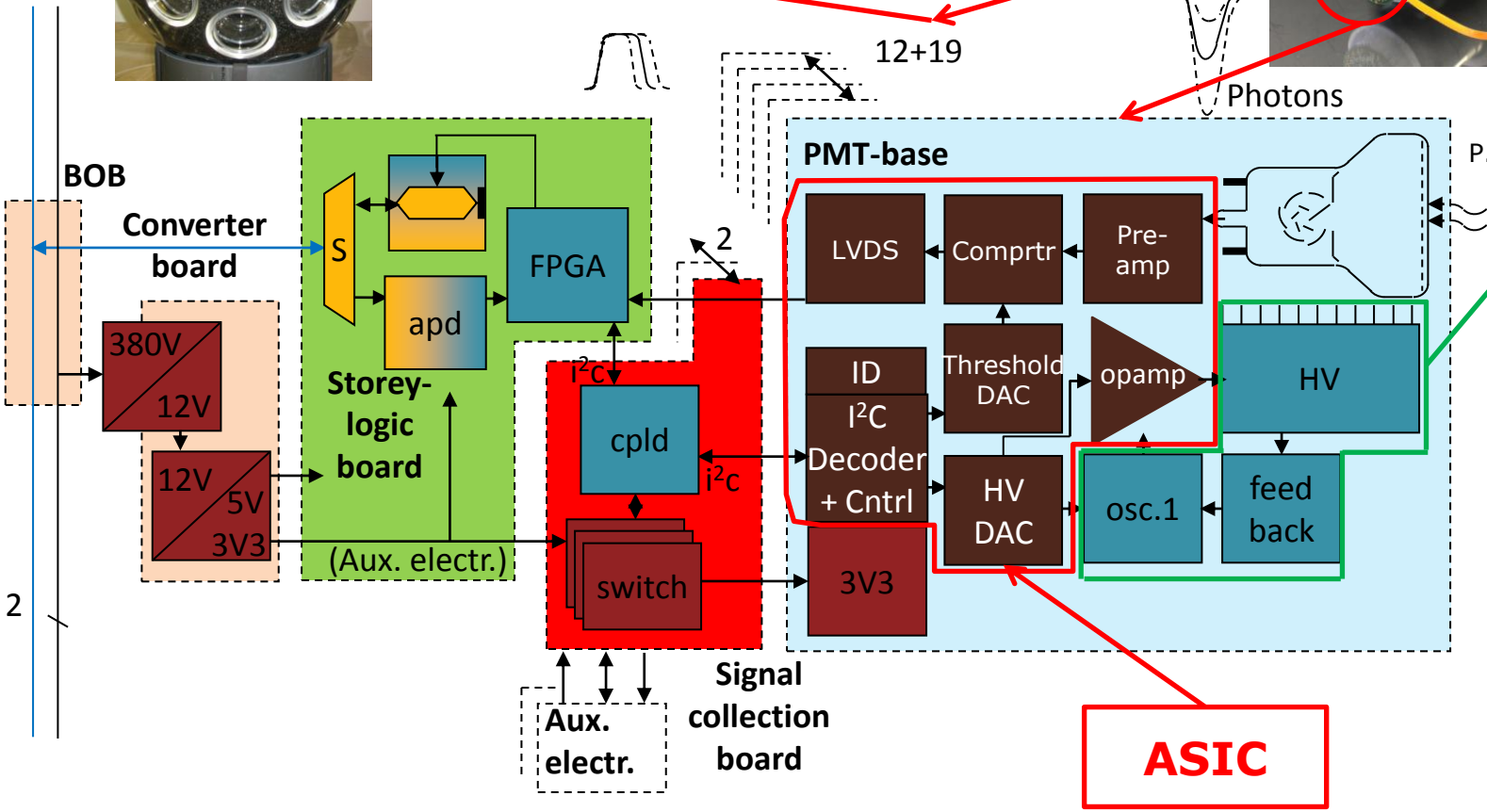




Read-Out Electronics

31 ASICs per Optical Module





Specifications of the ASIC

- Time resolution : 2ns (Photon arrival time accuracy)
- Time-over-Threshold : 1pe → 25ns (800 000 e^-)..10pe → 350ns (8000000e^-)
- Number of channels : several hundred thousands.
- LVDS signaling.
- I^2C slow control.
- Comparator threshold adjustment: 0…375 000 e^- → V_{in}^{com} = ±200mV
  Resolution : 8bits (bin size=1500 e^- / 1.2mV)
- Reference voltages for High Voltage circuit:

  2.0V …2.8V (resolution 8bits)→ High Voltage: -700V …-1500V
- Power consumption : ~ 20mW
- Technology: 0.35µm CMOS (AustriaMicroSystems)
- Immunity to dirty Power supplies
- Immunity to voltage breakdowns originated in the PMT

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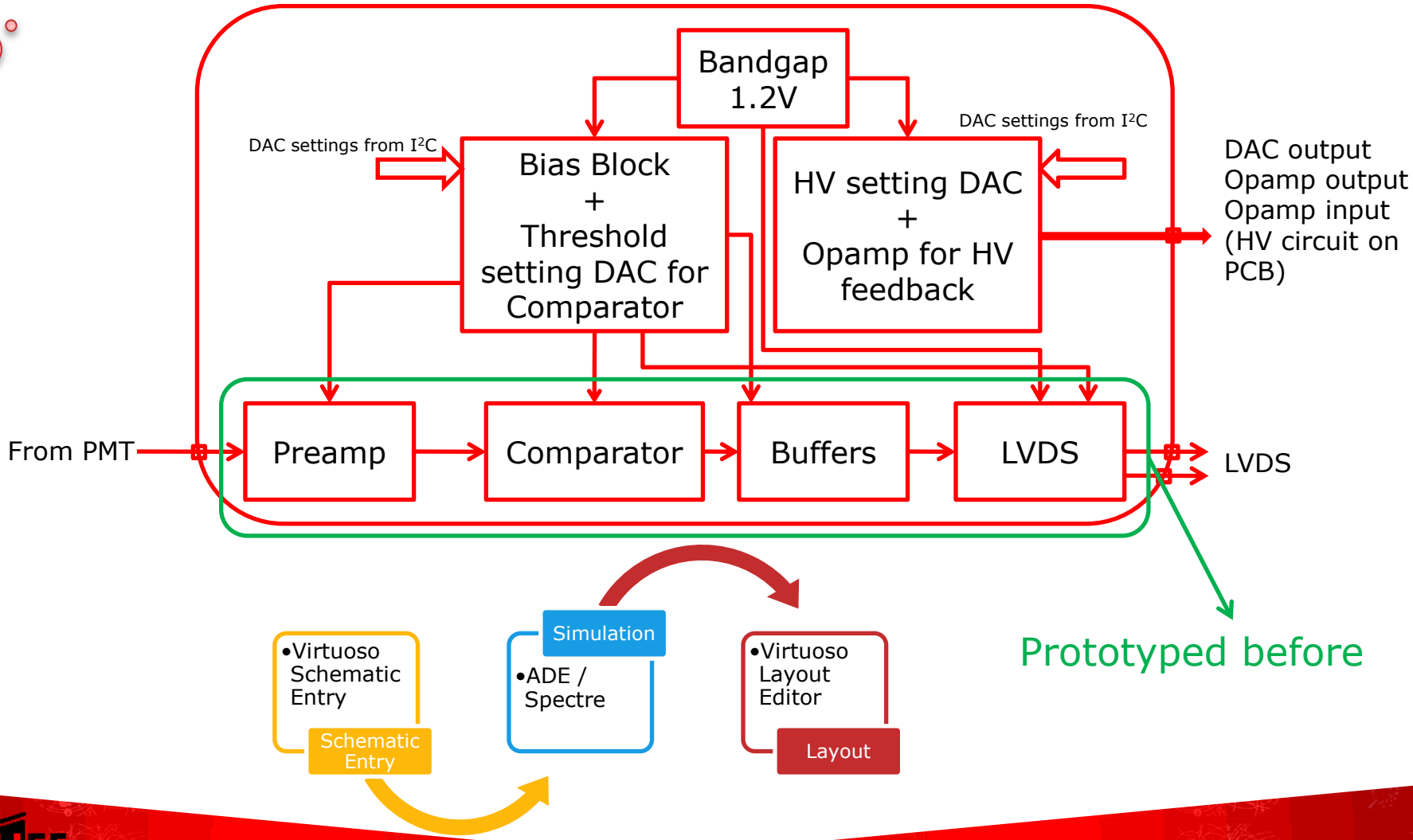
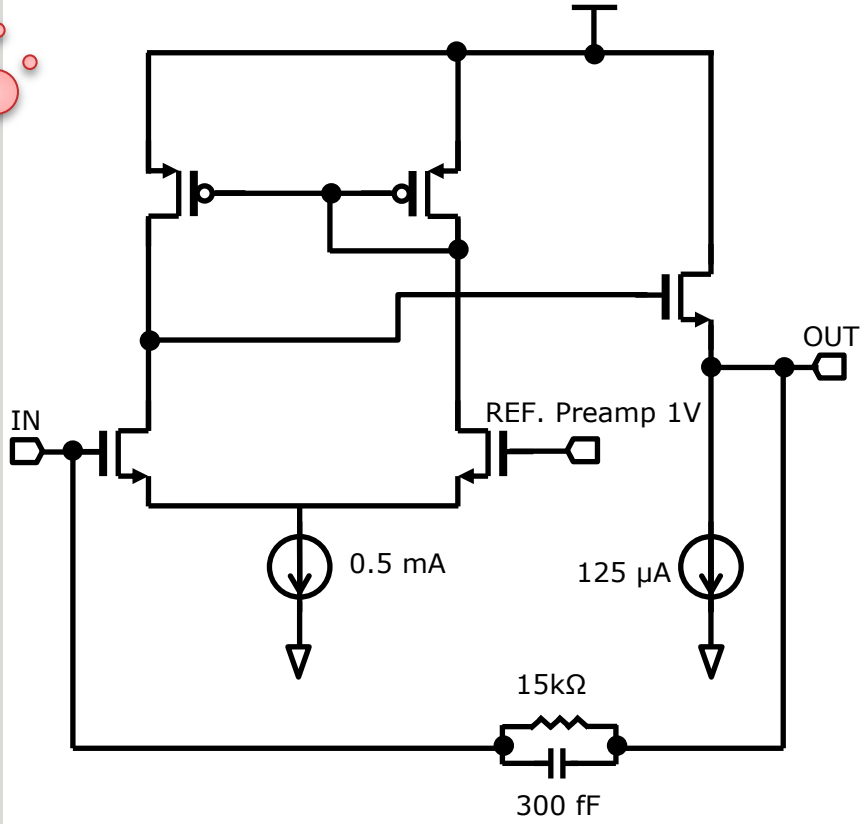
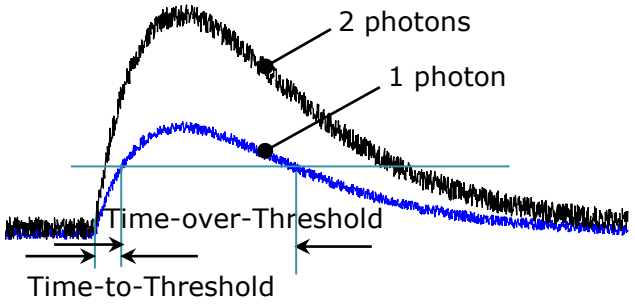
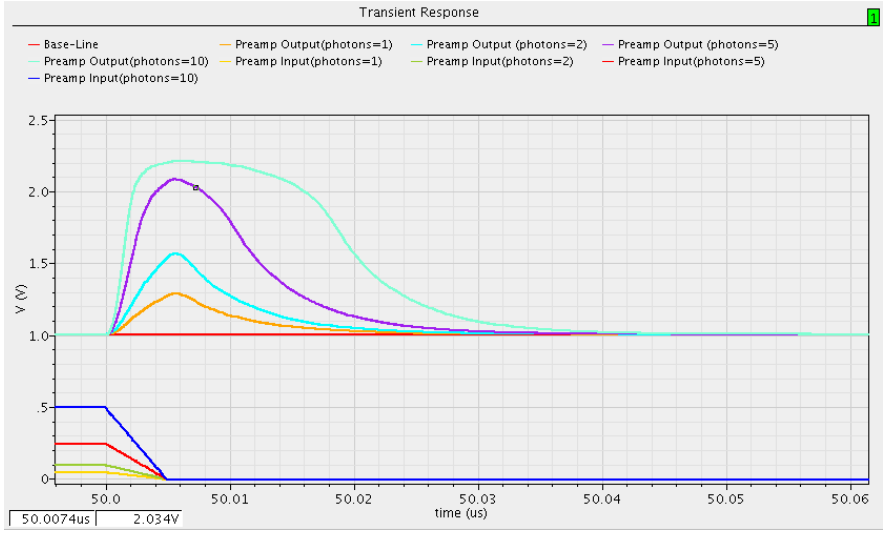
Analog Part


Bandgap
1.2V
DAC settings from I²C
Bias Block
+
Threshold
setting DAC for
Comparator
DAC settings from I²C
HV setting DAC
+
Opamp for HV
feedback
DAC output
Opamp output
Opamp input
(HV circuit on
PCB)
From PMT
Preamp
Comparator
Buffers
LVDS
LVDS
•Virtuoso
Schematic
Entry
Schematic
Entry
Simulation
•ADE /
Spectre
•Virtuoso
Layout
Editor
Layout
Prototyped before

Preamplifier

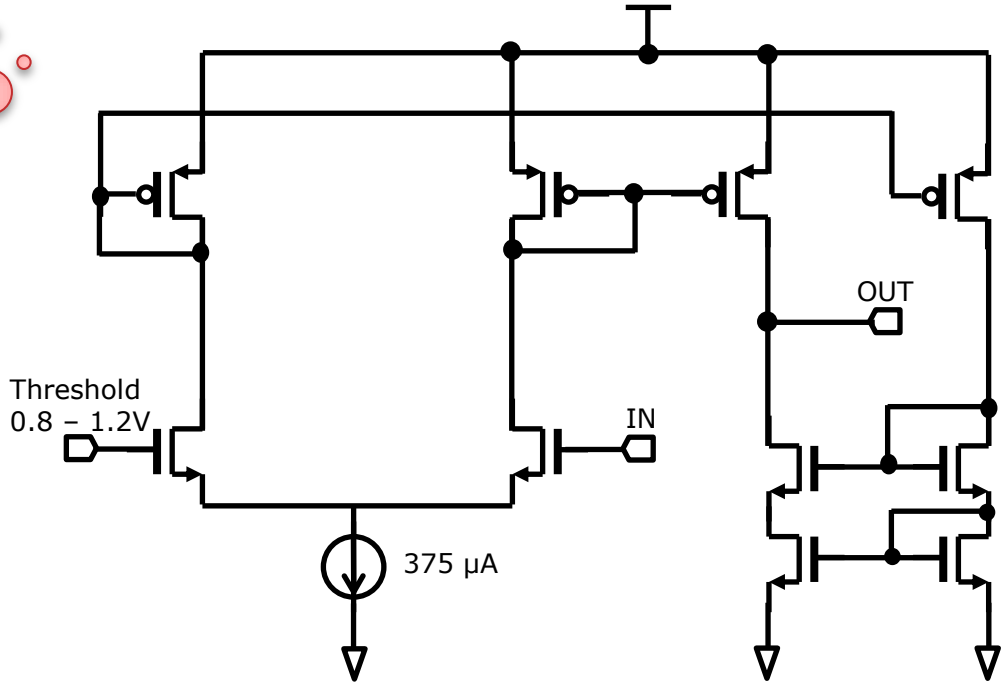


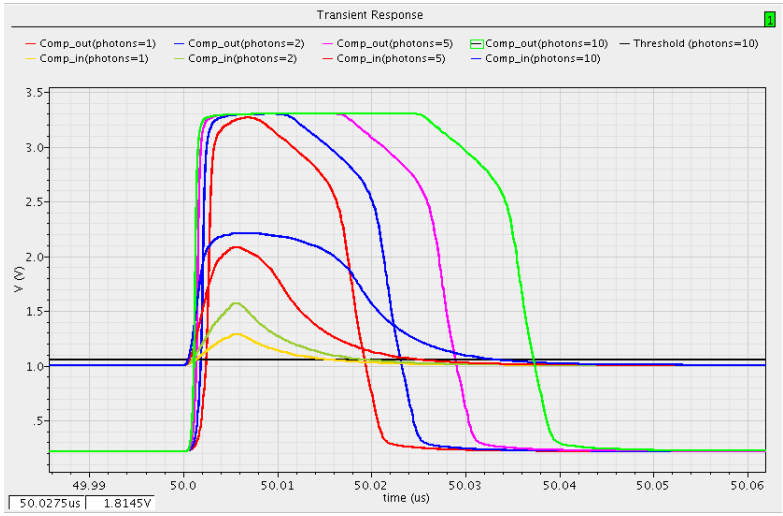




- Two-stage charge preamplifier with RC feedback.

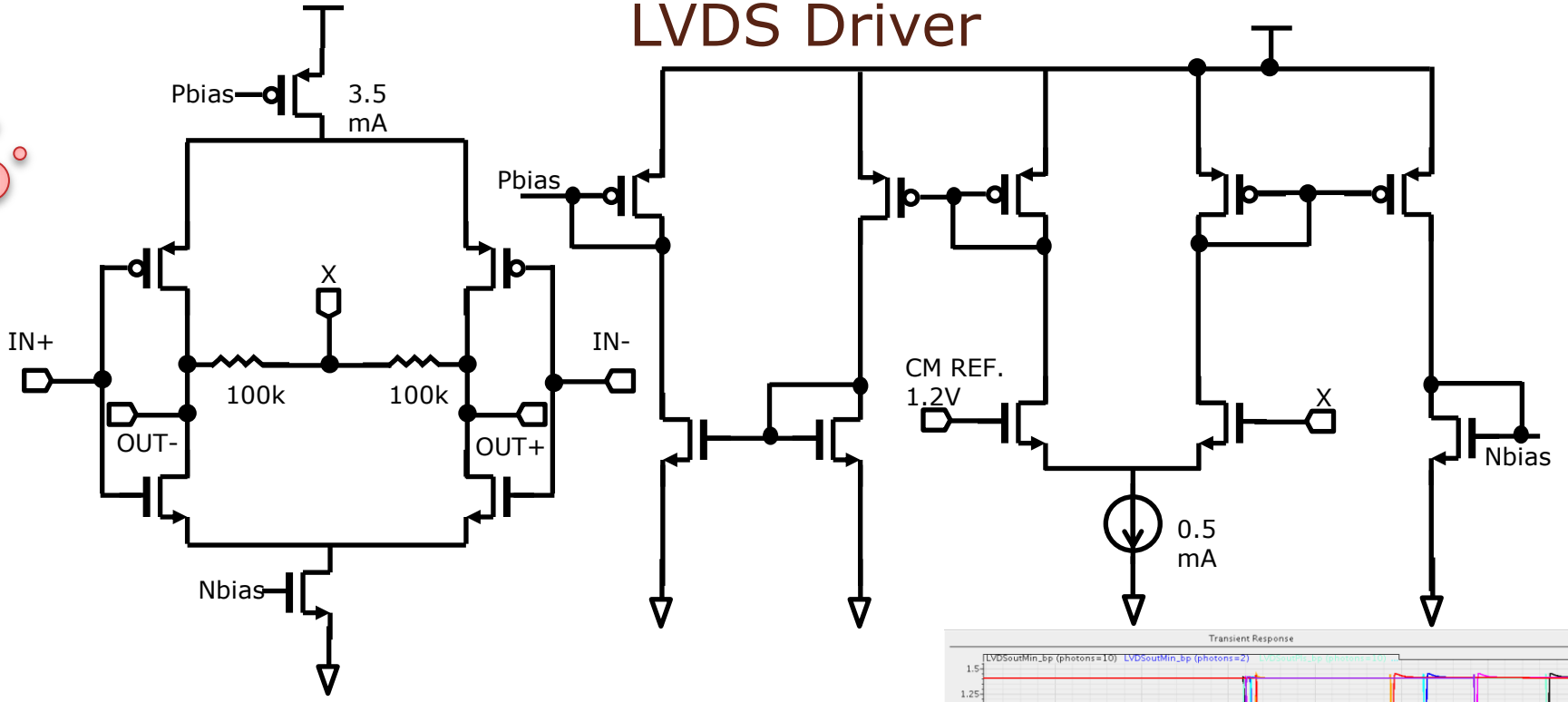
Comparator

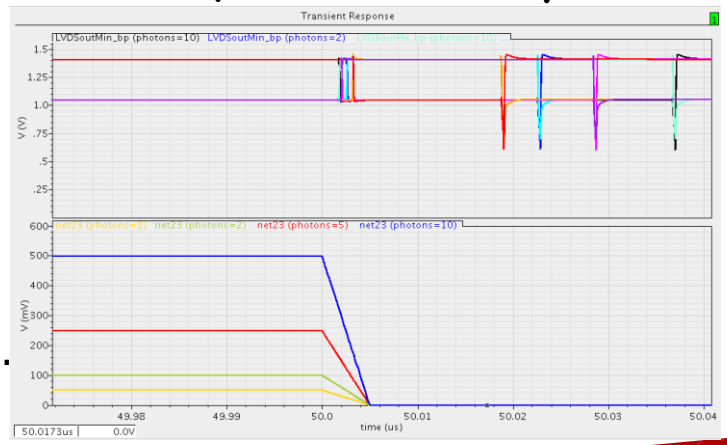




- Single Stage comparator.

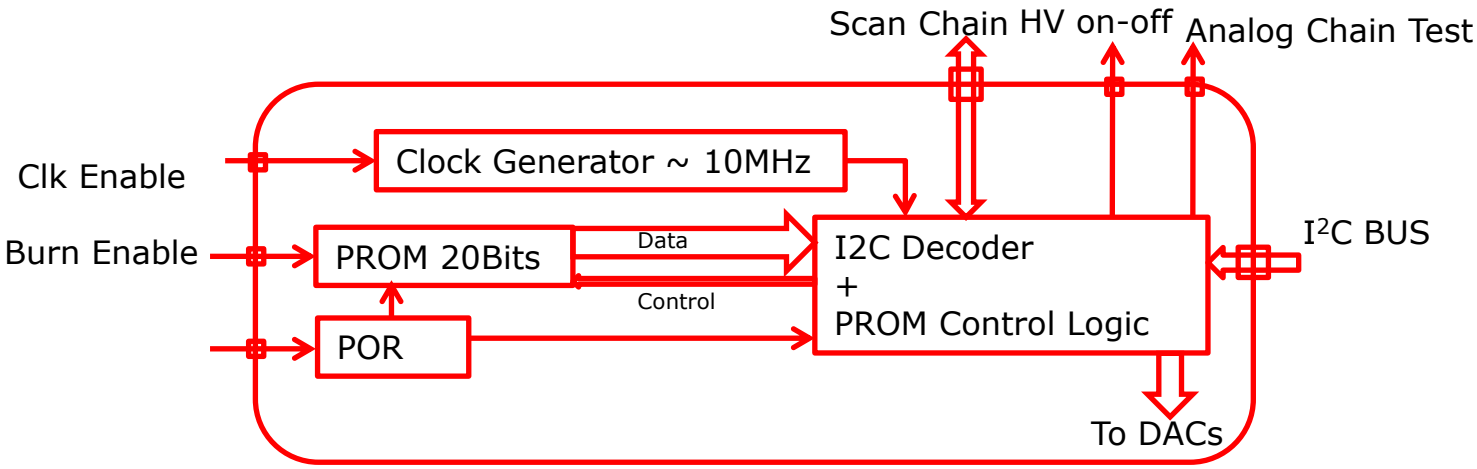
LVDS Driver

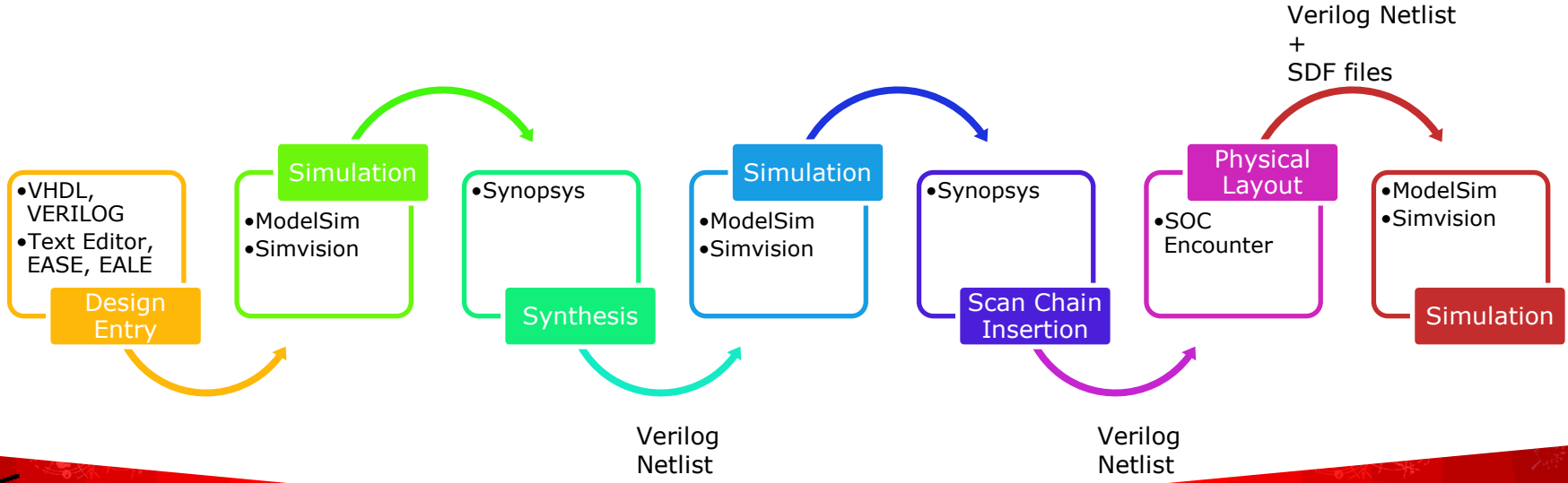




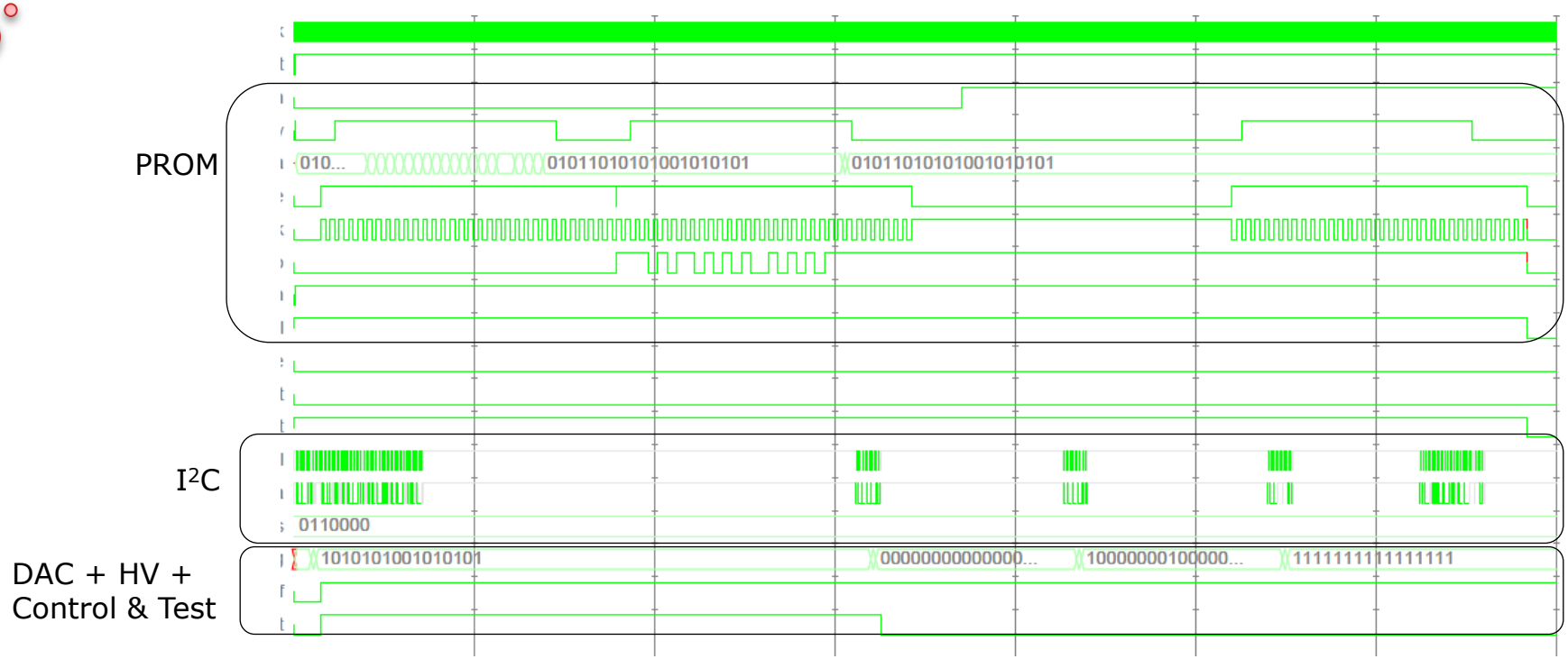
- Conventional LVDS driver, single stage CMFB circuit.
- 3.5mA * 100Ω = 350mV differential signal.

Digital Part



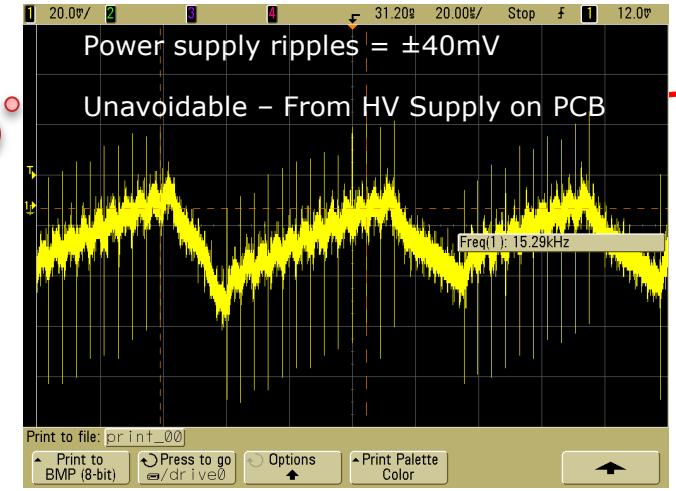


Digital Simulations - Example

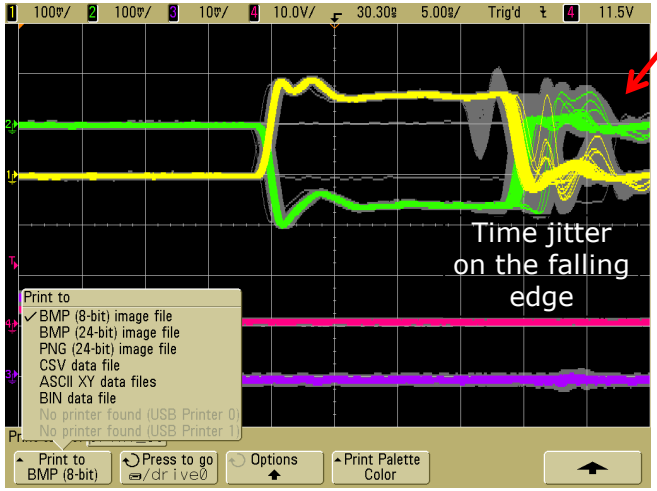


- Post Layout simulations with SDF files (Digital Part only).
- Tools Used : Modelsim, ncSim suite, Synopsys.

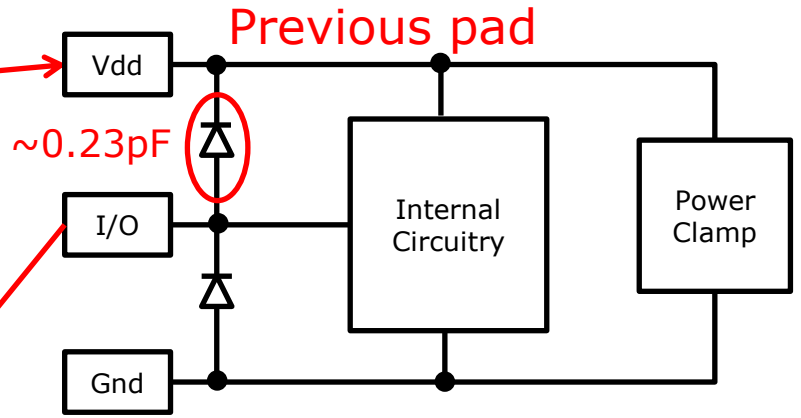
Analog Bondpad Modifications



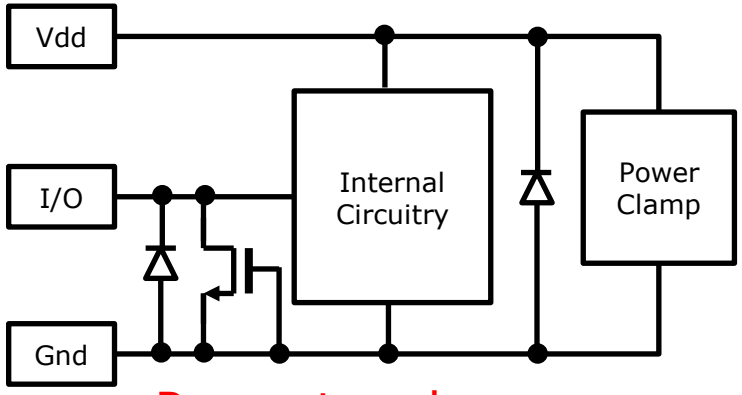
Problem



Previous pad

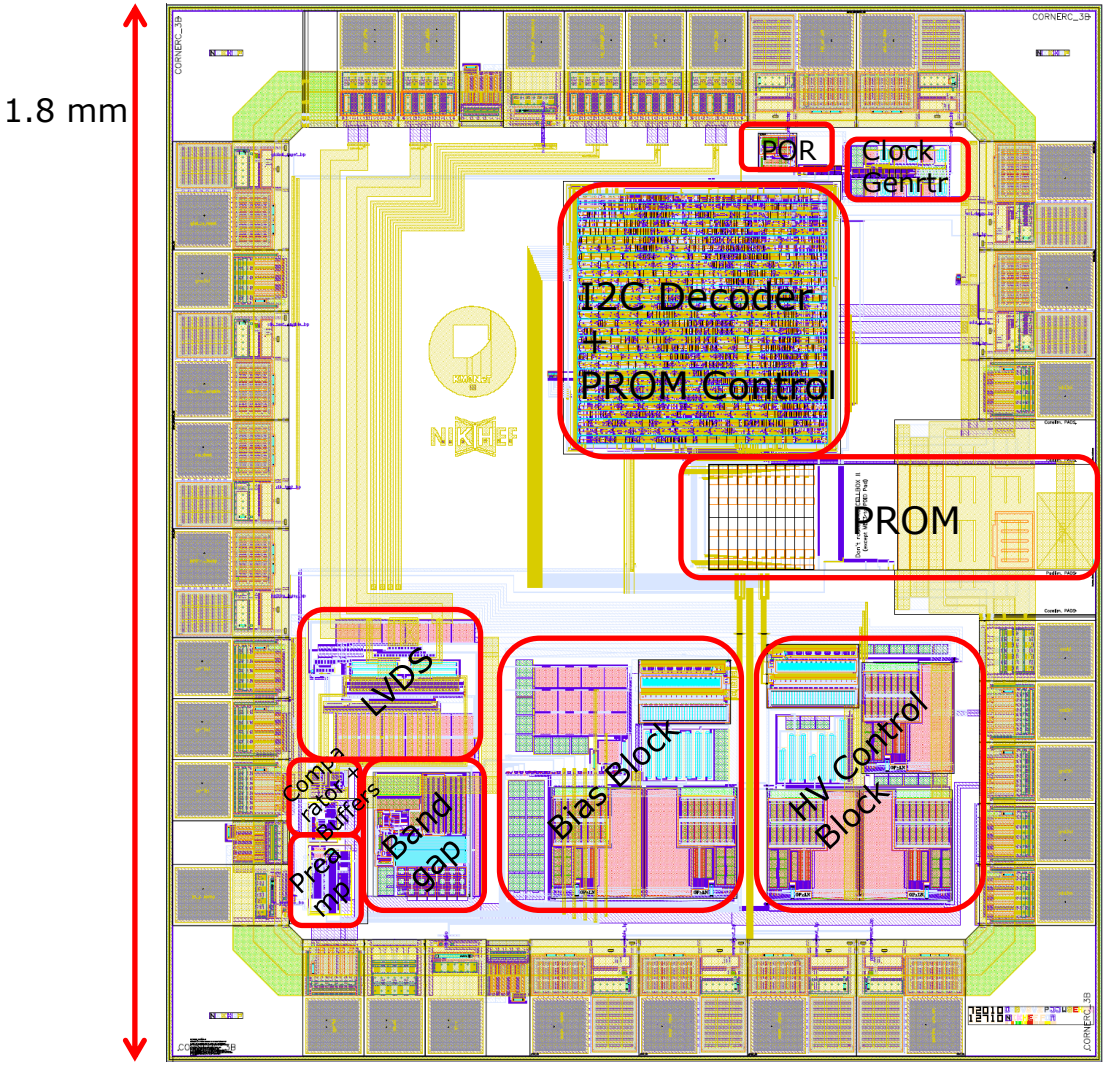


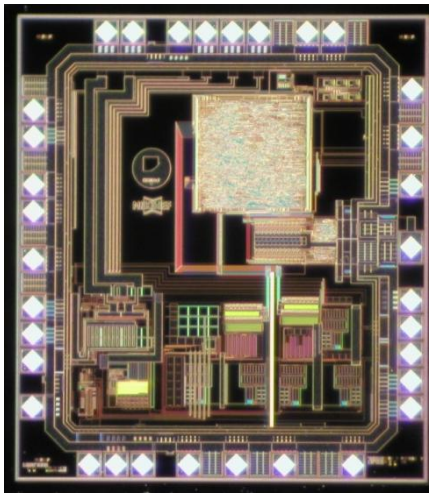
Possible Solution

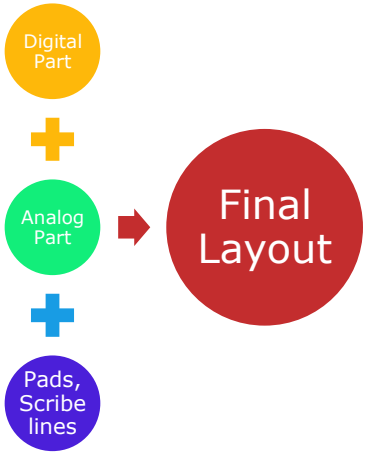


Present pad

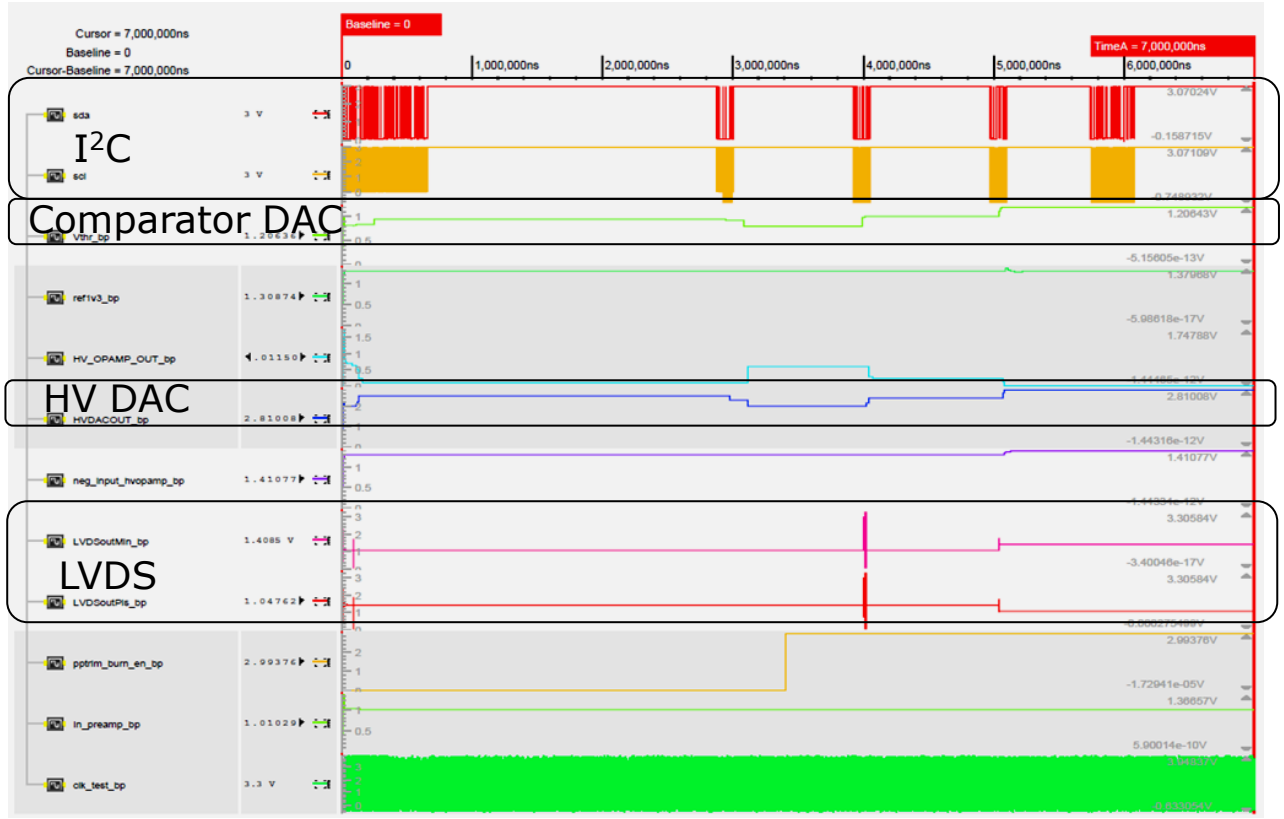
Layout & Integration

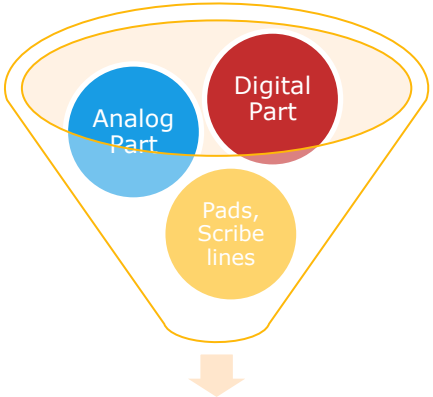






Mixed-Signal Simulation Results

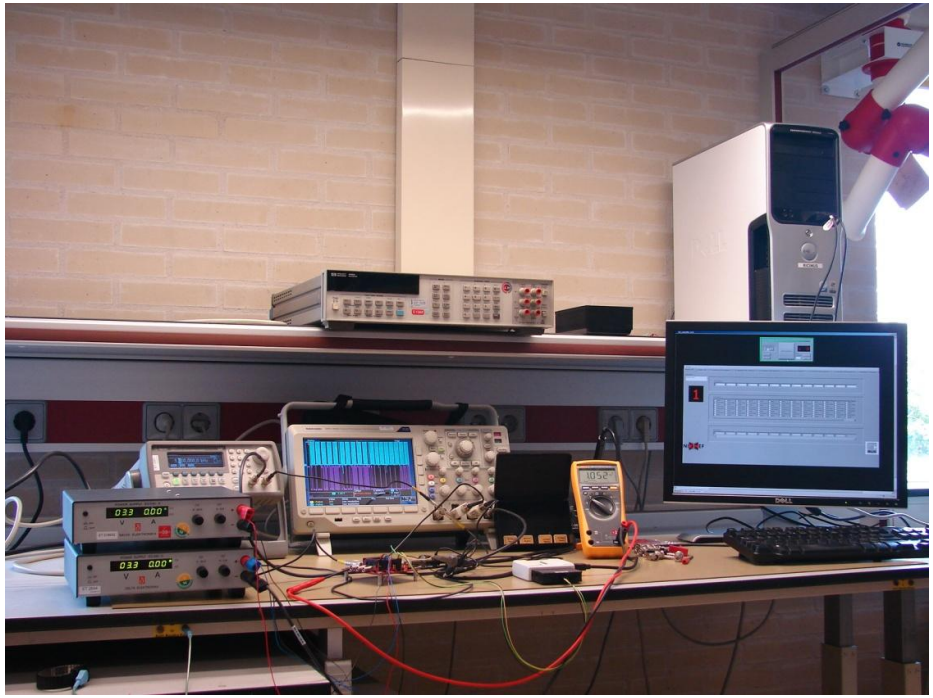


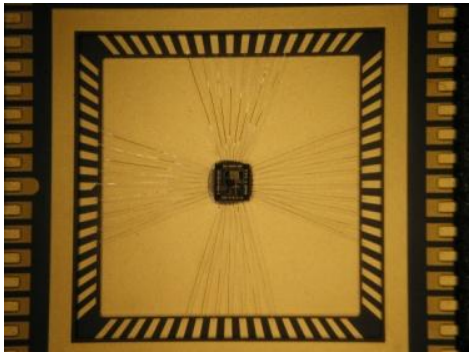


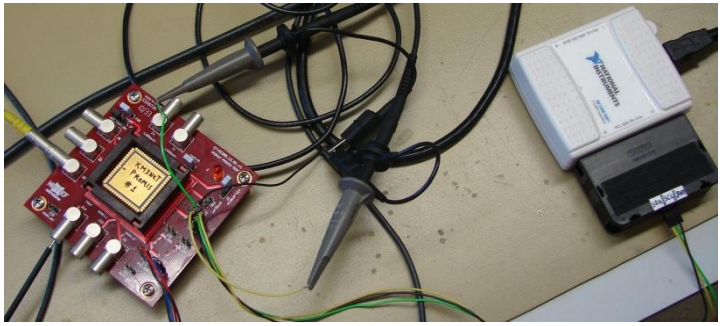
Final Simulation Results

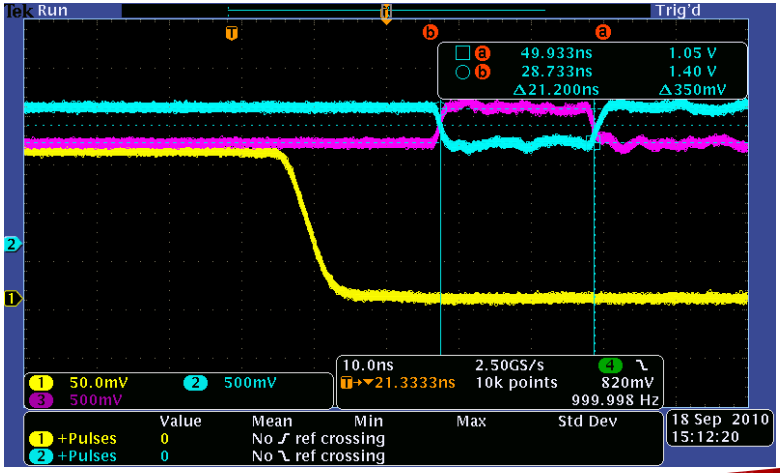
- Post Layout including Bondpads simulations.
- Tools Used : AMS environment (Ultrasim/spectre and ncSim suite).

Test Setup



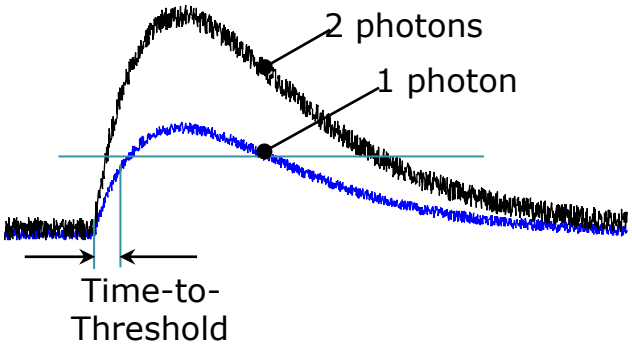


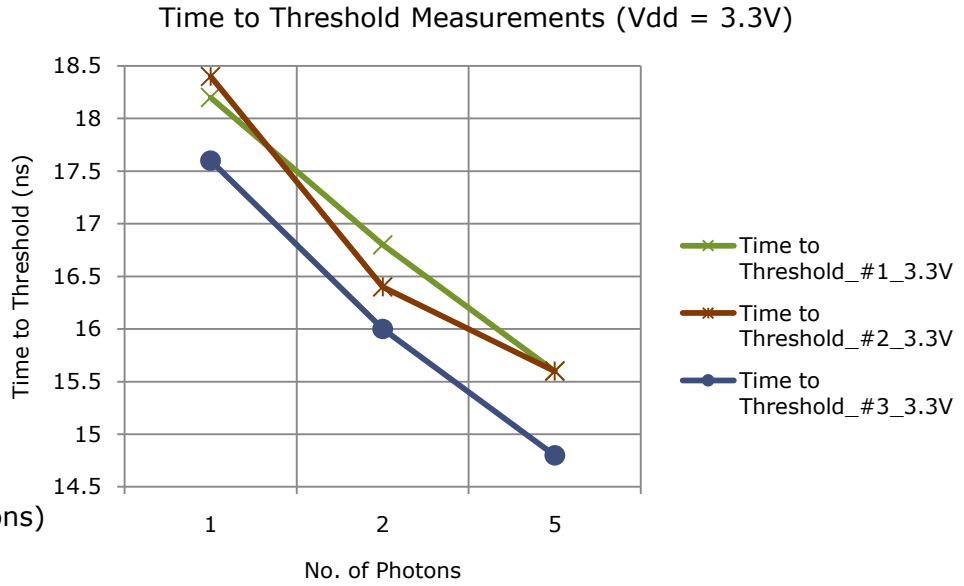


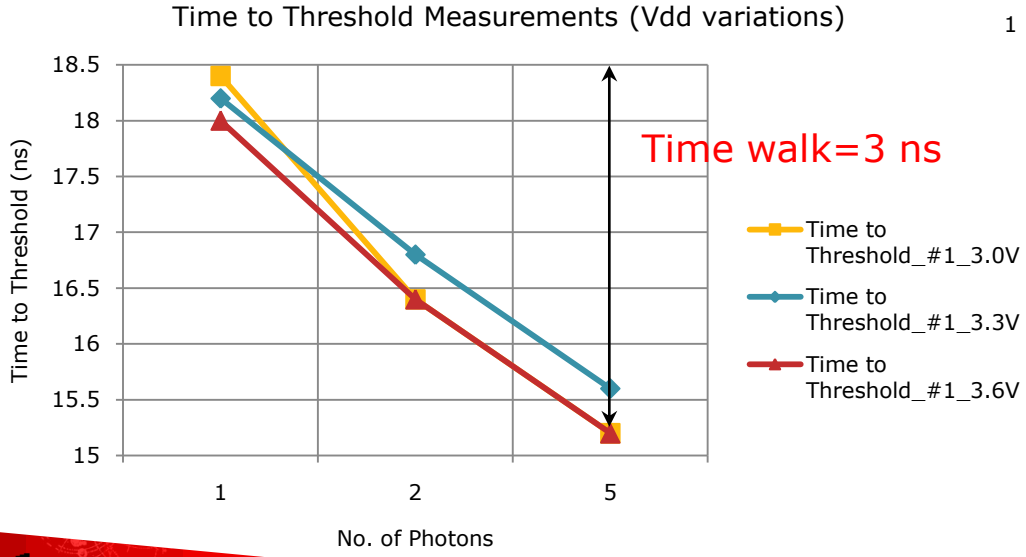


- Preliminary tests only.
- 3 samples packaged and tested.
- I^2C communication successful.
- DAC settings changeable.
- Analog chain functional.

Test Results







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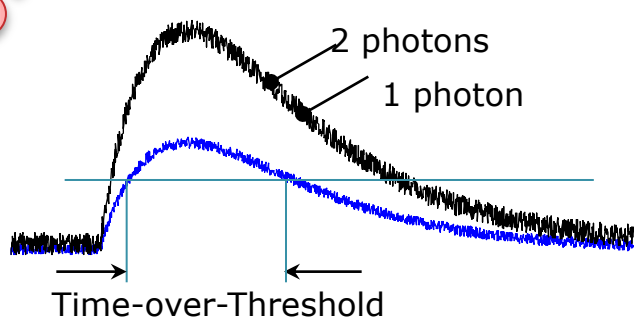

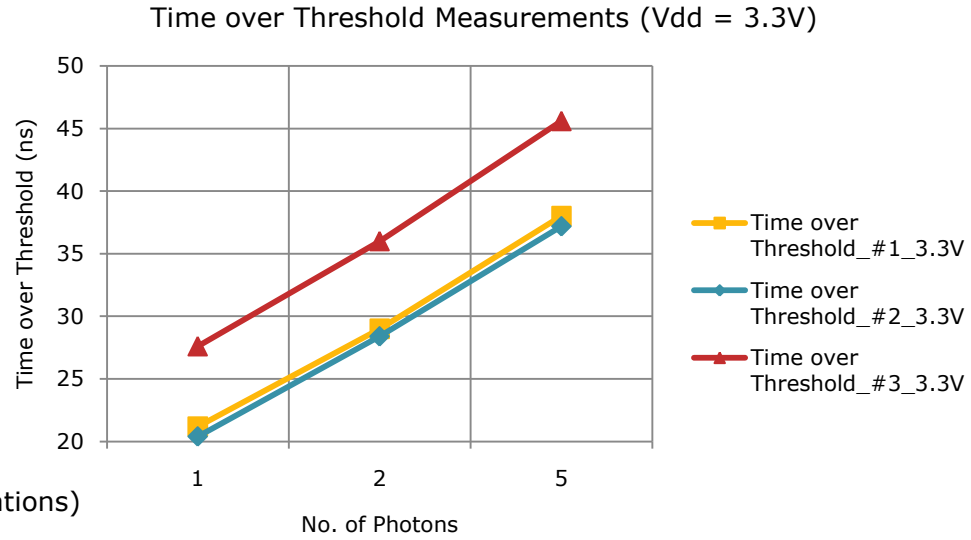

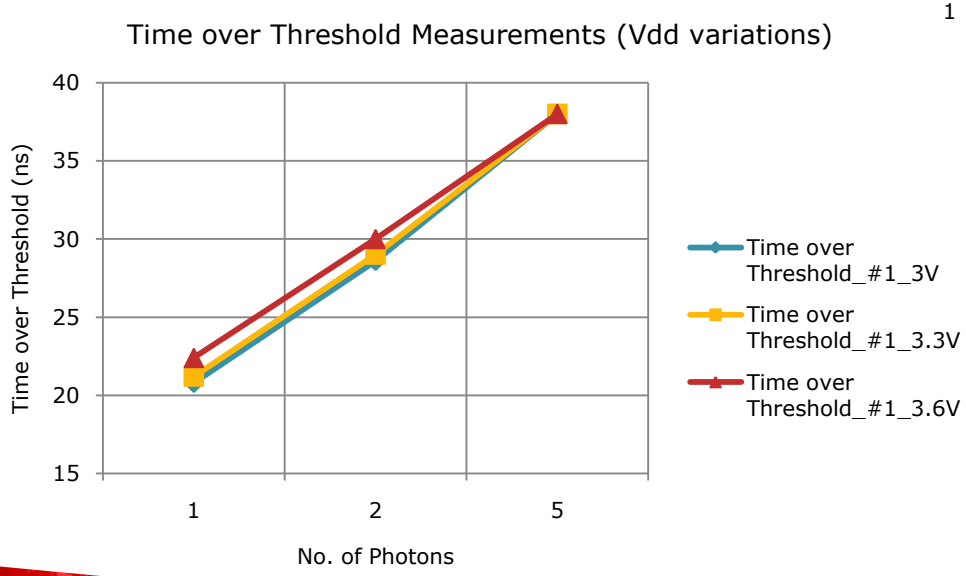

Conclusions & Future

- An ASIC to read out the PMT was successfully designed, simulated, fabricated and tested.
- Preliminary “Test results” are satisfactory & in line with simulation results and future functionality is being tested.
- More intensive tests need to be performed on the ASIC.
- We aim an engineering run during Q1 of 2011, allowing for a production ramp-up in Q1 of 2012.

Thank You

- KM3NeT project team, V. Gromov, Eric Heine, Ruud Kluit, John Hug, Jan-Willem Schmelling, P. Jansweijer, V. Zivkovic, P. Timmer, Joop Rovekamp, ET colleagues at NIKHEF.

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