Contribution ID: **59** Type: **Oral**

Study for the LHCb readout board

Wednesday, September 22, 2010 11:50 AM (25 minutes)

The LHCb experiment envisages to upgrade its readout speed from 1 MHz to 40 MHz. The consequence for the electronics is higher densities and an increase of serial links speed. Moreover the architecture must be reviewed to cope with links carrying data, clock and slow control at the same time.
Relying on boards compliant with the xTCA standard, we demonstrate how it is possible to build a flexible, scalable system consistent with the requirements. Measurements related to signal integrity, clock distribution and performance of the supervision system are also presented.

Summary

The LHCb experiment envisages to upgrade its readout electronics in order to increase the trigger speed from 1 MHz to 40 MHz. This electronics upgrade is very challenging, since readout boards will have to handle a higher number of links with an increased bandwidth. In addition, the new communication protocol introduced by the GBT chip mixes data acquisition, slow control and clock distribution on the same link, requiring new architectures as well as new efficient methods of control.

To explore the feasibility of such readout boards, an experimental system has been built around scalable reusable elementary building blocks. Their goals are multiple:
- understand signal integrity when using highly integrated high speed serial links (8.5 Gbits/s and above);
- test the implementation of the GBT protocol within FPGAs;
- understand advantages and limitations of commercial standard with a predefined interconnection topology;
- validate ideas on how to control easily such a system;
- check whether it is possible to distribute a clock with fixed and repetitive phase to front-end using high speed serial links and FPGAs.

We designed two boards compliant with the xTCA standard which meets an increasing interest in the physics community. These boards are:
- a generic AMC board handling 32 optical high speed serial links in or out;
- a communication switch mounted on a commercial MCH board allowing the AMC boards to communicate together.

In this presentation, we will describe jitter measurements obtained at 8.5 Gbits/s on serial link running the GBT protocol and their variation according to various parameters, as well as some simulations extrapolating these results to higher speeds.
We will illustrate the versatility of this architecture which can be tuned from basic acquisition systems (μTCA) to more high-end complex ones (ATCA).
A low cost scalable control system based on NIOS cores running from very simple servers in the early phases of the development to more complex μClinux/Dim/PVSS environments will be demonstrated.
And finally a few measurements will be shown concerning the phase distribution of a system clock transported on serial data after several serialization/deserialization stages through Stratix IV GX FPGAs.

Primary author: CACHEMICHE, Jean-Pierre (Centre de Physique des Particules de Marseille)

Co-authors: HACHON, Frédéric (Centre de Physique des Particules de Marseille); MARIN, Frédéric (Centre de Physique des Particules de Marseille); DUVAL, Pierre-Yves (Centre de Physique des Particules de Marseille); LE GAC, Renaud (Centre de Physique des Particules de Marseille)

Presenter: CACHEMICHE, Jean-Pierre (Centre de Physique des Particules de Marseille)

Session Classification: Systems, planning, installation, commissioning and running experience

Track Classification: Systems. Planning, installation, commissioning and running experience