Contribution ID: **55** Type: **Poster**

Upgrade of the PreProcessor System for the ATLAS Level-1 Calorimeter Trigger

Thursday 23 September 2010 16:00 (2 hours)

The ATLAS Level-1 Calorimeter Trigger is a hardware-based pipelined system designed to identify high-pT objects in the ATLAS calorimeters within a fixed latency of 2.5us. It consists of three subsystems: the PreProcessor which conditions and digitizes analogue signals and two digital processors. The majority of the PreProcessor's tasks are performed on a dense Multi-Chip Module(MCM)consisting of FADCs, a time-adjustment and digital processing ASICs, and LVDS serializers designed and implemented in ten years old technologies. An MCM substitute, based on today's components (dual channel FADCs and FPGA), is being developed to profit from state-of-the-art electronics and to enhance the flexibility of the digital processing. Development and first test results are presented.

Summary

The ATLAS Level-1 Calorimeter Trigger is a hardware-based pipelined system designed to identify high-pT objects in the ATLAS calorimeters within a fixed latency of 2.5us, including all transmission delays. The real-time path in the trigger is subdivided into three stages. The PreProcessor which conditions and digitizes 7200 pre-summed analogue signals from the calorimeters is followed by two subsequent object-finding digital processor systems working in parallel: the Jet/Energy-sum processor and the Cluster Processor. It provides all the calorimeter based trigger information used by the Central Trigger Processor to make the final Level-1 trigger decision.

The PreProcessor is a compact, highly modular system with the majority of the processing performed on a dense Multi-Chip Module(MCM) which handles four input channels and consists of nine unpackaged dies: four FADCs, a time-adjustment ASIC with 1ns resolution, a PreProcessor ASIC, and three LVDS serializers. The PreProcessor ASIC is a complex pipelined digital processing element which converts the digitized input signals into correctly time-aligned, calibrated and noise-suppressed outputs and assigns the energy deposits to the correct LHC bunch-crossing.

The basic MCM technology decisions have been taken a decade ago. At that time it was not feasible to have standard, packaged and really flexible components which would correspond to all requirements. The pin-, size- and latency-compatible substitute for the MCM based on today's components is being developed to profit from the exponential growth of state-of-the-art electronics. Full compatibility with the current module allows transparent replacement within the existing concept of the PreProcessor mother- and daughter-cards as well as mixed operation when old and new MCMs are used on the same board.

Two dual channel 105MHz FADCs AD9218 are used for compact, packaged, fast, low noise, low power digitization. A Xilinx Spartan-6 FPGA serves as a flexible, low-cost, configurable digital processing unit which replaces not only the PreProcessor ASIC but the time-adjustment chip and LVDS-serializers as well. A high degree of adaptability provided by the FPGA could be used for an adaptation of the digital processing algorithm if it will be required for a smooth operation after the LHC upgrade for the high luminosity.

Standard components allow us to use commercially available evaluation boards, together with the existing equipment for the current MCM

testing, for the FPGA configuration bitstream development and for tests in parallel with the design of the PCB layout for the new module.

Results of the development and first tests are presented in this work.

Primary author: KHOMICH, Andrei (Kirchhoff-Institut fuer Physik, Heidelberg University)

Presenter: KHOMICH, Andrei (Kirchhoff-Institut fuer Physik, Heidelberg University)

Session Classification: POSTERS Session

Track Classification: Trigger