

GOSSIPO-3: Measurements on the Prototype of a Read-Out Pixel Chip for Micro-Pattern Gas Detectors

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GOSSIPO-3 is the demonstrator of a front-end chip for the read-out of Micro Pattern Gas Detectors designed in IBM 130 nm CMOS in collaboration of Nikhef and the Physics Department Bonn.

The prototype features charge sensitive amplifiers, discriminators, a high resolution Time to Digital Converter, Low Drop Out voltage regulators for supply voltage control of the TDC, biasing circuits and control logic on a $2 \times 1 \text{ mm}^2$ die. It can be operated in a time measuring or an event counting mode. Following the prototype announcement at the TWEPP 2009, measurement data on noise performance, channel to channel gain, ToT spread and LDO load step response are now available.

Summary

Shortly after its announcement at the TWEPP 2009 in Paris, GOSSIPO-3 entered production. GOSSIPO-3 is a prototype of a front-end pixel chip for position-sensitive Micro Pattern Gas Detectors with $60 \times 60 \mu\text{m}^2$ pixels for high granularity. The front-end demonstrator can operate in 24 bit event counting mode or in time recording mode allowing measurements with a target precision of 1.7 ns (bin size) and a dynamic range of 102 μs for the arrival time. The target specifications for the Time over Threshold (ToT) measurements are an accuracy of 25 ns (corresponding to $\sigma = 200e^-$) and a ToT range of up to 6.4 μs . The target noise performance of the Charge Sensitive Amplifier (CSA) is $\text{ENC} = 70e^-$ (input equivalent) and a rise time of less than 20 ns. The goal for the power consumption is 3 $\mu\text{W}/\text{channel}$. The chip has been implemented in close collaboration of Nikhef (Amsterdam) and Physics Department Bonn (Bonn). The chip is designed in an 8 metal layer IBM 130 nm standard CMOS technology available through MOSIS.

The demonstrator comprises a complete pixel cell with analogue front-end circuits including biasing plus an on-pixel high resolution Time to Digital Converter (TDC), counters and control. The frequency of the ring-oscillator in the TDC can be tuned by regulating the supply voltage of the Voltage Controlled Oscillator (VCO). This is done with the help of a Low Drop-Out voltage regulator (LDO). Two alternative circuits for this LDO have been implemented. In addition to these circuits, three CSAs with constant current feedback each followed by a discriminator have been implemented. The CSAs share a common charge injection pad for testing. The outputs of all three discriminators are externally available through buffers. The comparator thresholds can be globally tuned on-chip by a 4-bit Digital to Analogue Converter. One of the CSA outputs is also buffered and available on a test pad. Besides these pixel related circuits, there is an InGrid Preamplifier (IP) on the demonstrator. When the final front-end chip is used in gaseous detectors with InGrid electron amplification stage, the IP is meant to deliver valuable information on charge injections on the amplifying grid. The inputs of the CSAs are protected from high-voltage breakdown between chip surface and InGrid by an especially designed protection device and a SiNitride protection layer on top of the die.

The "S3 Multi IO Board" designed by Physics Department Bonn and well-known in the pixel detector community is used for the read-out of the digital counter logic. First measurements on the preamplifier indicate a noise performance of the CSA well below $\text{ENC} = 70e^-$. First ToT measurements show good linearity but a channel-to-channel spread of about 45%. On-going analyses trace the fluctuation back to variations of the discharge feedback current of the CSA.

Both LDO test circuits take less than 5 ns to re-settle (accuracy 2%) after a current load step of 20 mA which is expected to be the average load step from average to peak activity for a detector consisting of 256×256 pixels with 240 active pixels per bunch crossing.

In autumn 2010 further measurement results and analyses will be available.

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