Displacement damage studies of power LDMOS devices for DC-DC conversion

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Outline

- Motivation
- LDMOS devices from IHP SGB25V GOD technology
- Neutron irradiations
- Additional gamma irradiations
- Other studies
- Conclusions

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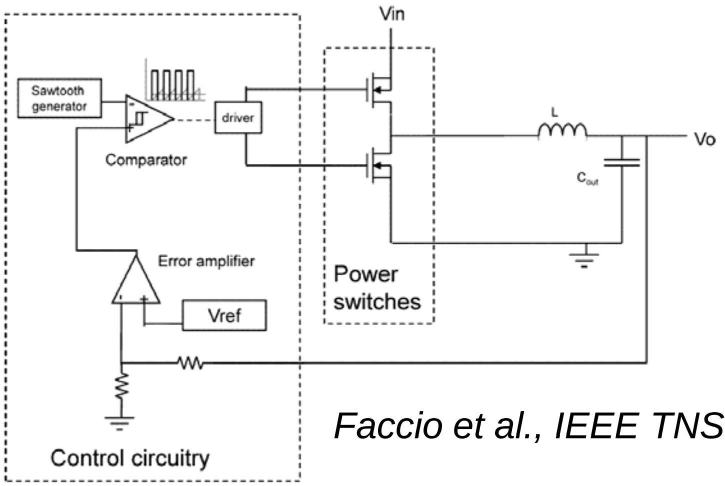
Motivation

- DC-DC powering for strips
  - Laterally Diffused MOS (LDMOS) devices constitute the power switches in buck converters:
    - Very high cut-off frequency, low losses (low R_{ON})
    - Implemented into standard (Bi)CMOS technologies (easier than VMOS)

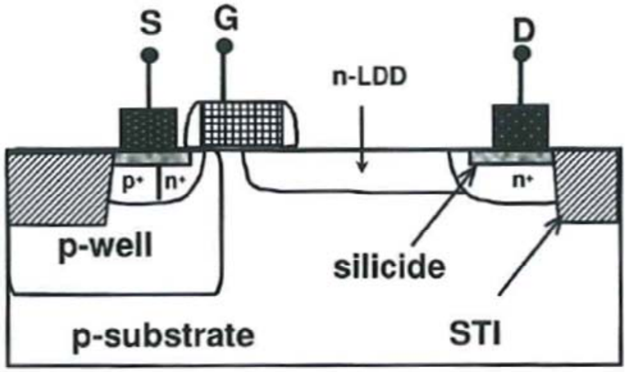


Faccio et al., IEEE TNS, 2010

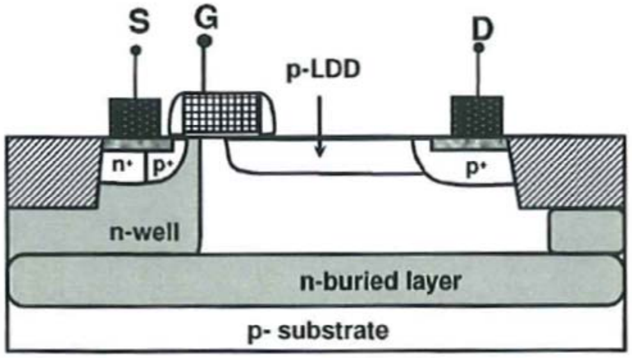
- Radiation tolerance must be investigated
  - Displacement damage investigated with neutron irradiations (complementary to F. Faccio studies, X-rays, p)

LDMOS devices from IHP

- **2^{nd} generation** devices from **IHP GOD** module (**G**ate **O**verlapped **D**rift)
  - Implemented on *0.25 µm SGB25V* SiGe BiCMOS technology from IHP Microelectronics
  - NLDMOS and PLDMOS devices:
    - L_{ch} x W_{ch} = 2x (**0.6**x5) µm^2 (drawn)
    - L_{Drift} = **0.6** µm (real)
    - T_{OX} ~ 5 nm
    - V_{BR} = 22 (-16) V
    - f_T = 20 (10) GHz
    - R_{ON} = 5 (12) Ω·mm
    - V_T = 0.6 (-0.53) V



NLDMOS



PLDMOS

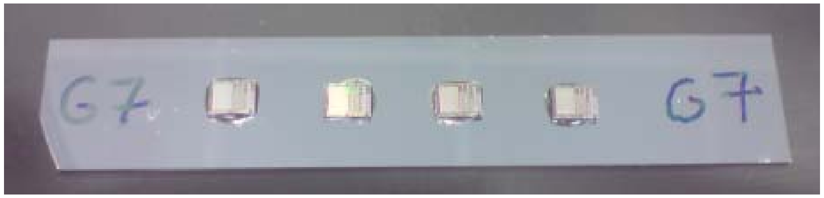
Radiation damage mechanisms

- Nonionizing radiation damage:
  - Atomic displacement
    - Vacancies, interstitials, divacancies, impurity atoms,...
    - DEFECTS on the silicon crystalline lattice = energy levels in the bandgap
      - Thermal generation of e/h pairs via midgap levels
      - Thermal recombination of e/h pairs via midgap levels
      - Scattering centers for carriers
      - Others: type inversion, transient capture of carriers,...

    - “Bulk” effect
    - Normally of secondary concern for MOS devices
    - May be important for LDMOS devices due to the drift region

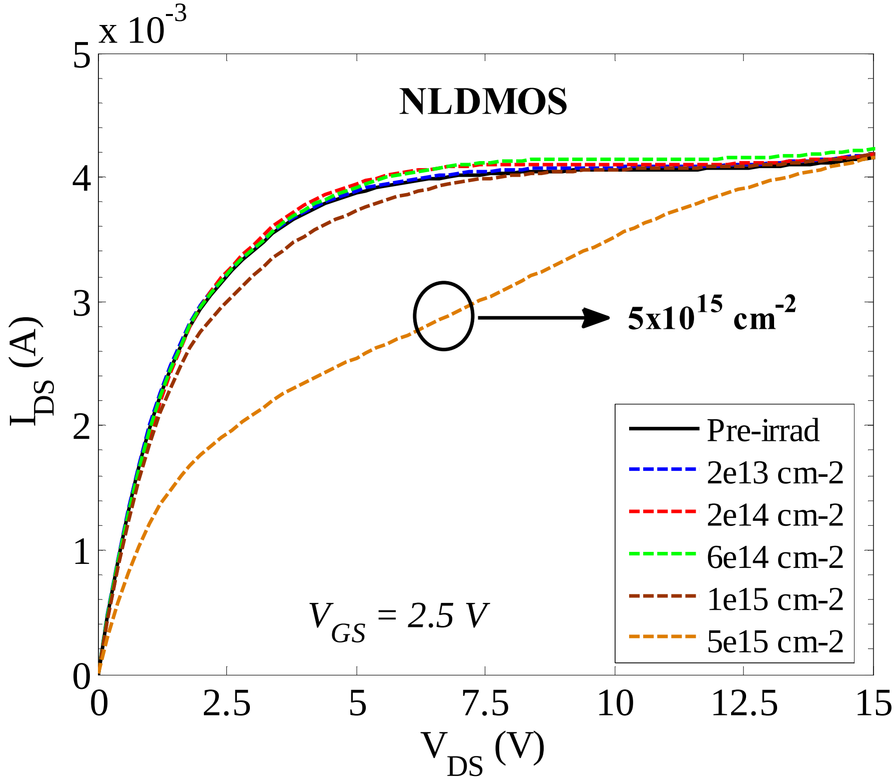
Experiment

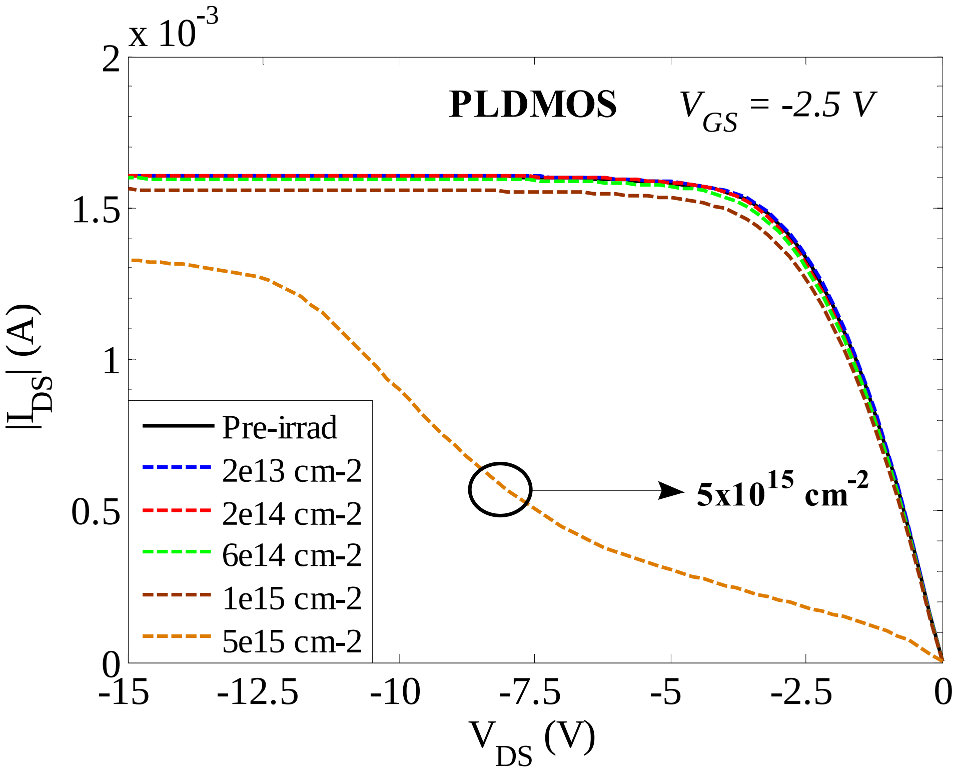
- Neutron irradiations (atomic displacement damage)
  - *TRIGA* nuclear reactor at *JSI*, Ljubljana
    - 2×10^{13}, 2×10^{14}, 6×10^{14}, 1×10^{15}, 2×10^{15}, 4×10^{15}, 5×10^{15} cm^{-2} (1 MeV n_{eq})
    - *“Parasitic” Total Ionizing Dose (TID)*: 100 krad(Si) per every 10^{14} n_{eq}/cm^2
    - Cd shield to avoid thermal neutrons
    - 4 devices per type and fluence
    - Devices with terminals floating during irradiations
    - Annealing: several measurements at RT + **7 days @ 100ºC**



Results (neutron irrads)

- $I_{DS}(V_{DS})$ curves @ V_{GS} = 2.5 V

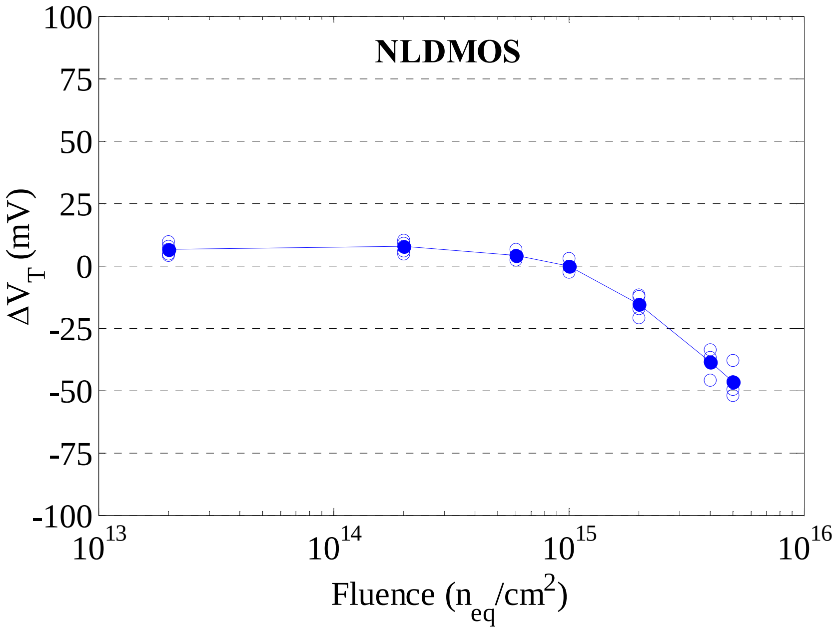


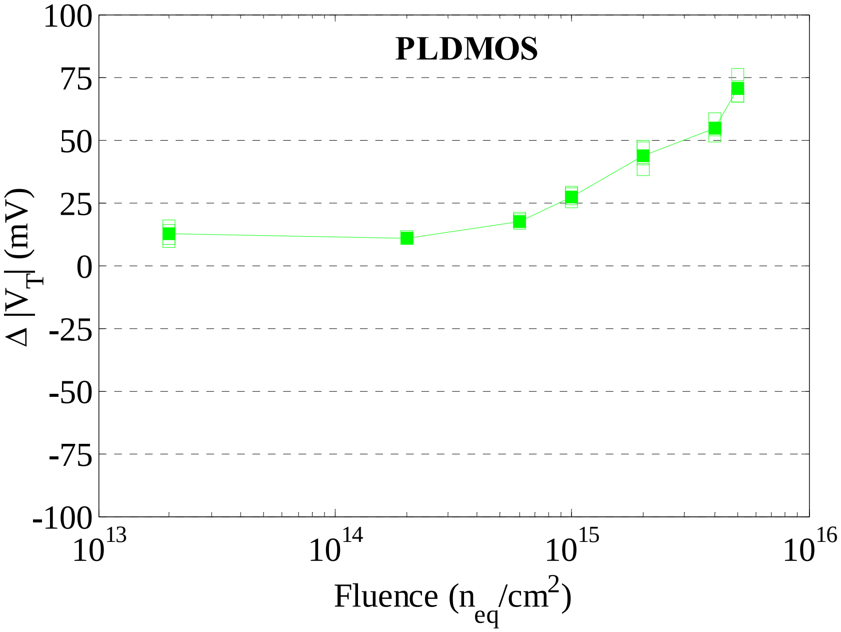


  - Very small changes up to 1x10^{15} n_{eq}/cm^2

Results (neutron irrads)

- Threshold voltage shift: **$\Delta|V_T| = |V_{Tf}|-|V_{T0}|$** (@ V_D = 50 mV)





  - Max ~ -50 mV for NLDMOS
  - Max ~ 70 mV for PLDMOS
  - Mostly related to TID (1-5 Mrad(Si) for 1x10^{15}- 5x10^{15} cm^{-2})
    - Oxide charges + interface traps: initial decrease for NLDMOS, monotonic V_T increase for PLDMOS

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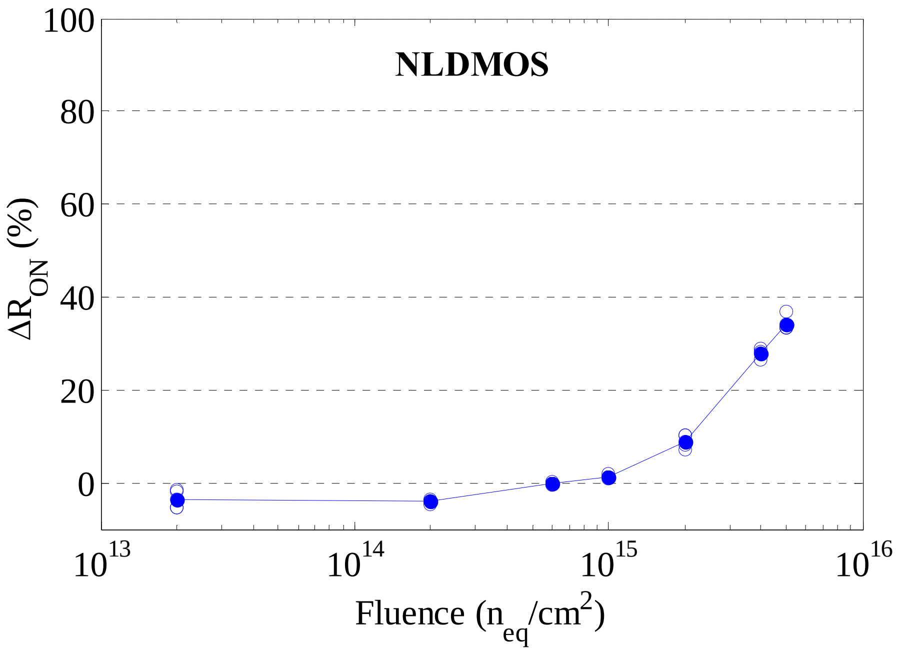
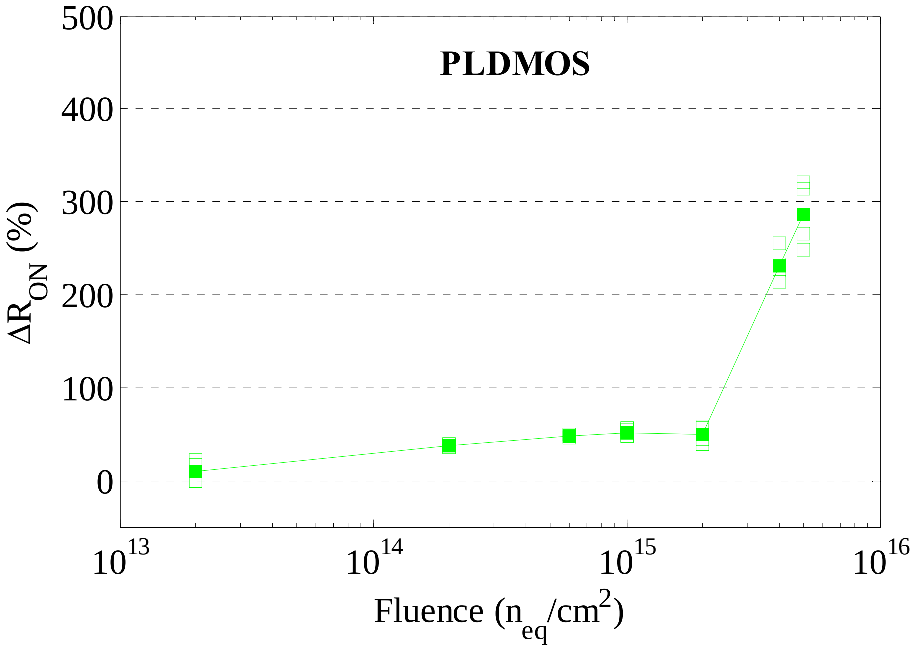
Results (neutron irrads)

- On-resistance variation: **ΔR_{ON} = (R_{ONf} -R_{ON0}) / R_{ON0}** (%)





  - Max ~ 35 % for NLDMOS
  - Max ~ 300 % for PLDMOS
  - Main effect of displacement damage
    - Scattering centers in the drift region
      - Decrease of carriers mobility => Increase of R_{ON}

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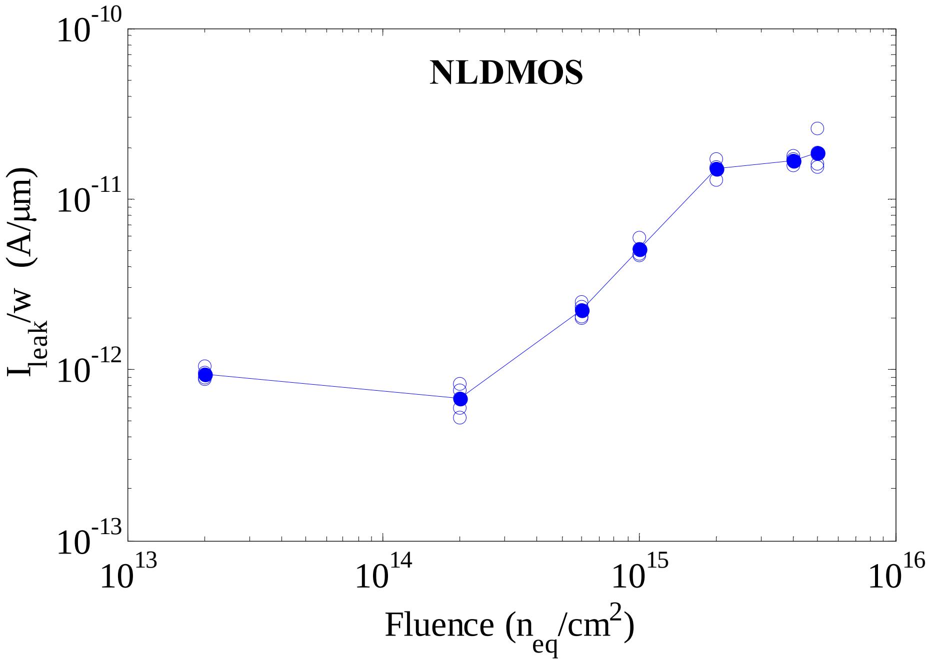
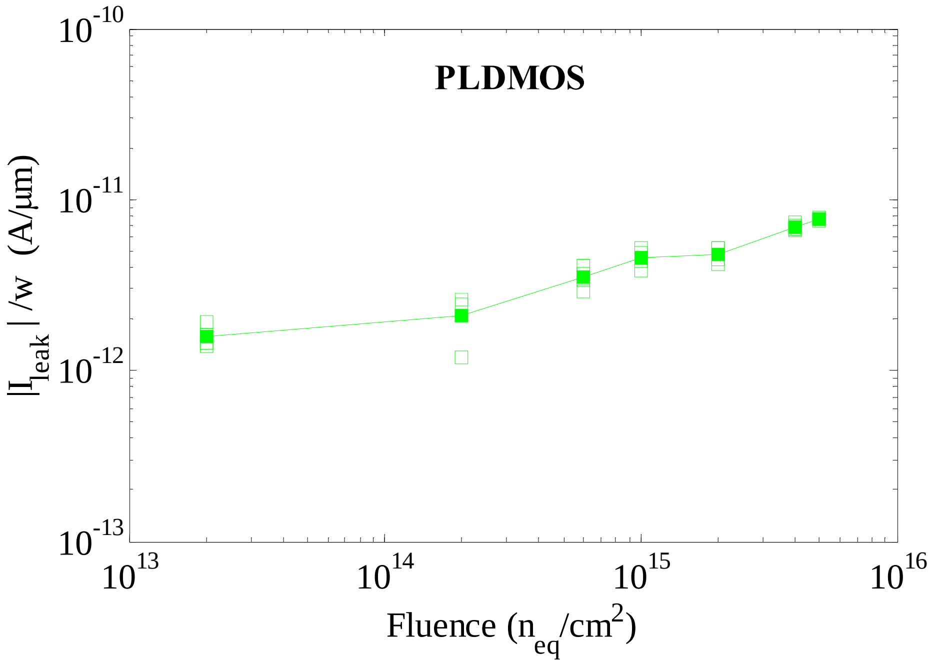
Results (neutron irrads)

- Leakage current density: $\mathbf{I_{leak}/w}$ (@ $V_{GS} = 0$, $V_D = 15$ V)





  - Observable increase of I_{leak}
  - Max < 0.1 nA/µm both for NLDMOS and PLDMOS
    - Related to thermal generation of e/h pairs via near-midgap levels induced by atomic displacement

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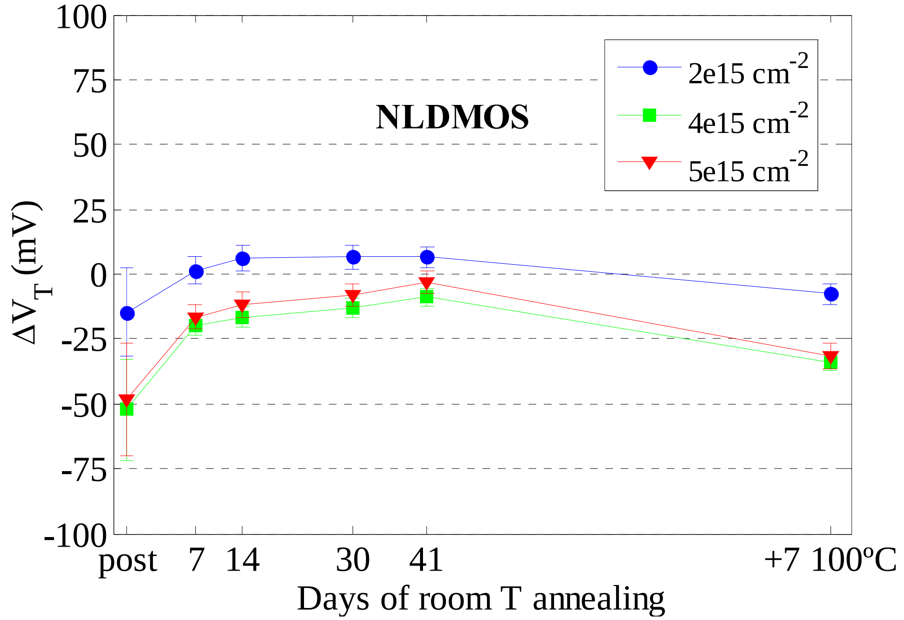
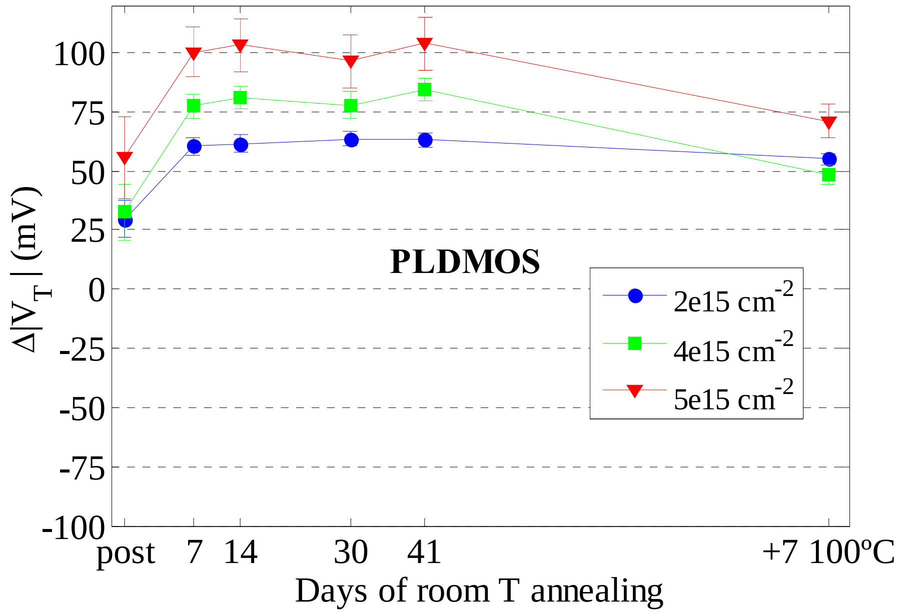
Results (neutron irrads)

- Annealing:
  - 2×10^{15}, 4×10^{15} and 5×10^{15} n_{eq}/cm^2
  - Devices with terminals floating (same condition as irradiation)
  - ~ 41 days @ RT (5 measurements)
  - + 7 days @ 100°C

Results (neutron irrads)

- Annealing: $\boldsymbol{\Delta|V_T|}$ = $|V_{Tf}|-|V_{T0}|$ (@ V_D = 50 mV)





- Little changes of V_T
- Expected behavior for ionizing radiation damage
  - Partial annealing of oxide traps, increase of interface traps
    - ΔV_T less negative for NLDMOS
    - V_T more negative for PLDMOS

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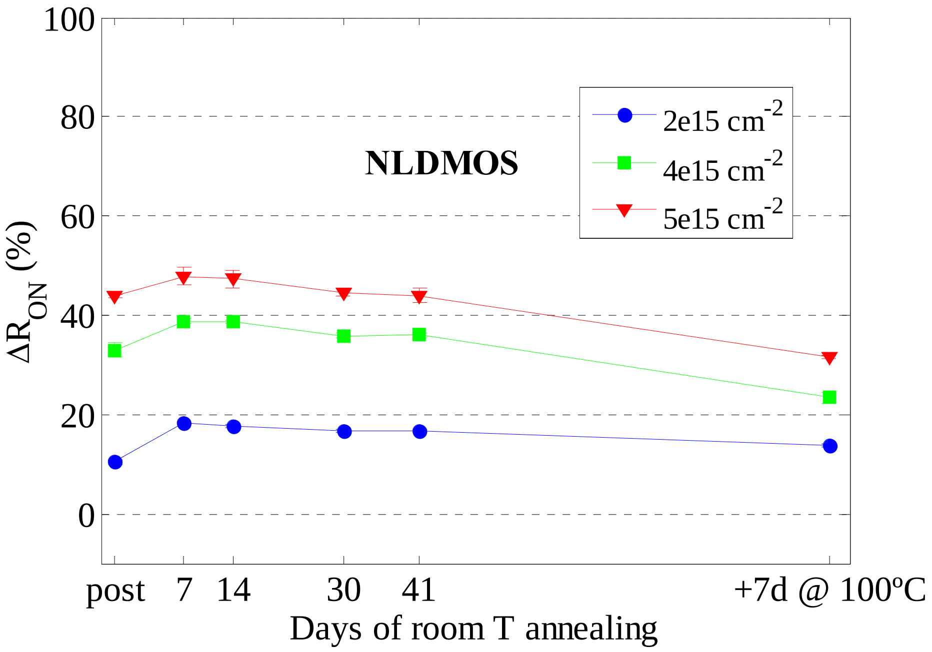
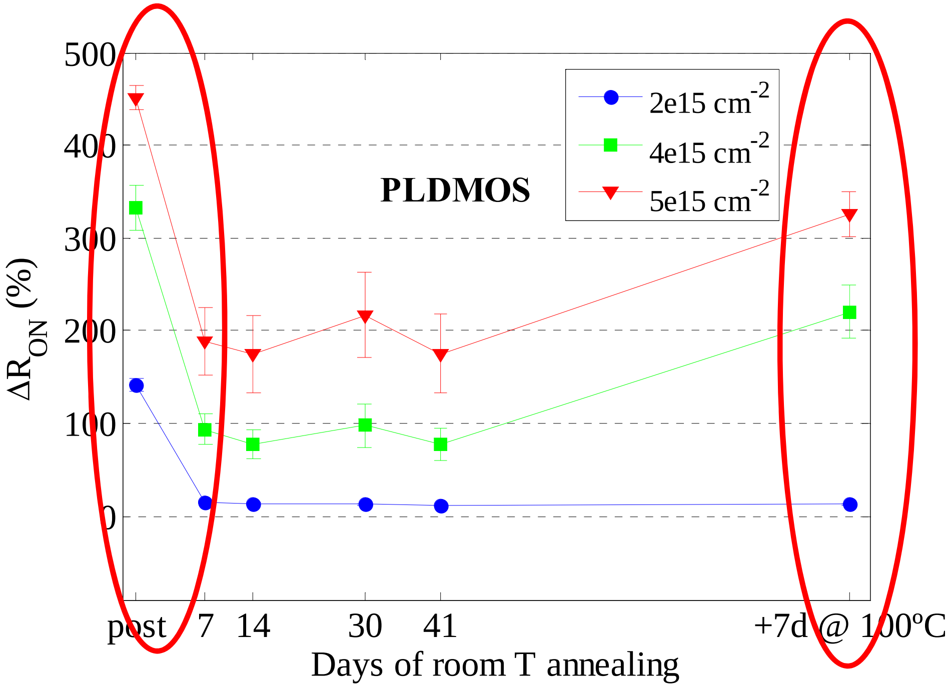
Results (neutron irrads)

- Annealing: $\mathbf{\Delta R_{ON}} = (R_{ONf} - R_{ON0}) / R_{ON0}$ (%)

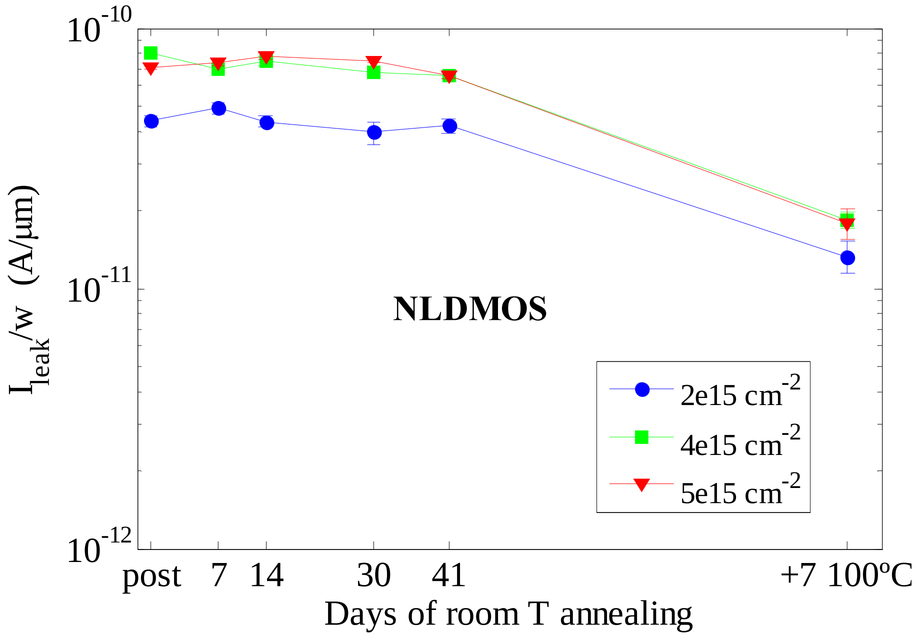


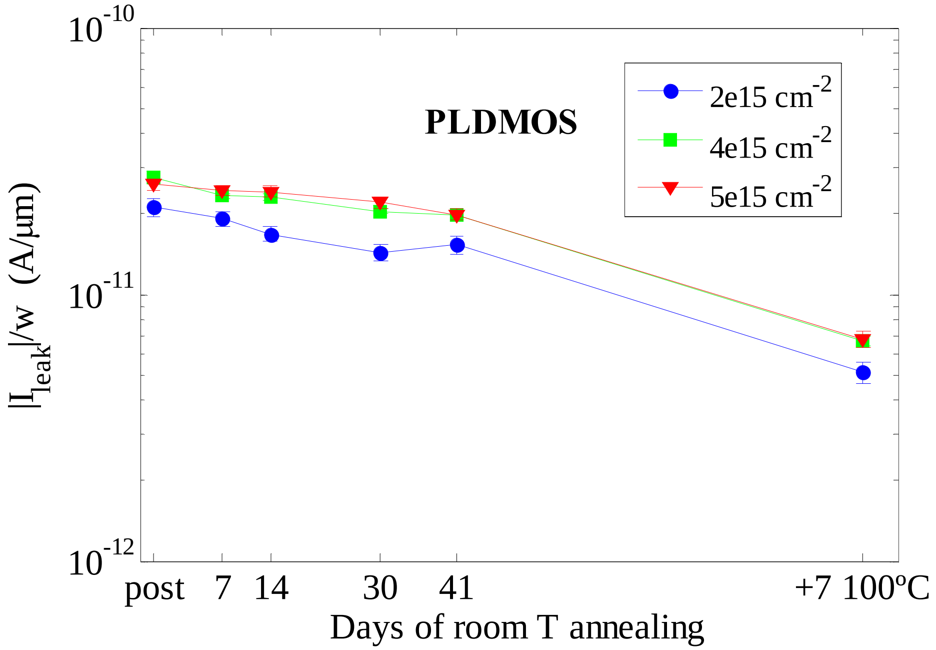


  - Little changes of R_{ON} for NLDMOS, as expected, although visible initial change consistently observed w.r.t. post-irrad measurement
  - Anomalous evolution of R_{ON} for PLDMOS
    - Related to annealing dynamics of the radiation-induced defects producing scattering centers

Results (neutron irrads)

- Annealing: Leakage current (**I_{leak}/w**)





  - Decrease of I_{leak} both for NLDMOS and PLDMOS
    - Annealing of defects producing e/h generation in the channel region of the device

Additional gamma irradiations

- Motivation: Identify and separate ionizing and displacement damage from the neutron irradiations
- ^{60}Co source at CIEMAT, Madrid (NAYADE water-well source)
  - 0.65, 5, 10 Mrad(Si)
  - Devices with floating terminals (same as neutrons)
  - 4 devices per type and dose
  - Annealing: same to neutron irrads

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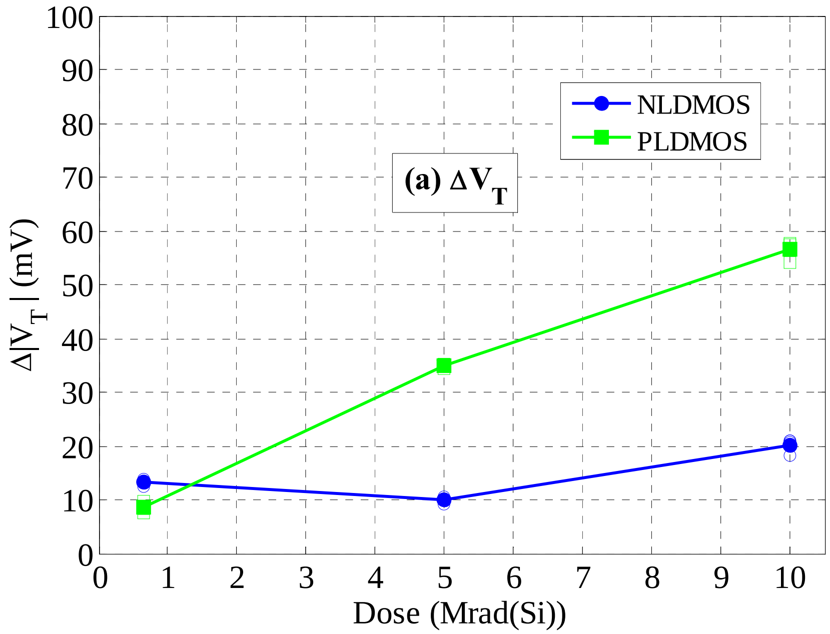
Results (gamma irrads)

- **$\Delta|V_T|$** = $|V_{Tf}|-|V_{T0}|$ (@ V_D = 50 mV)



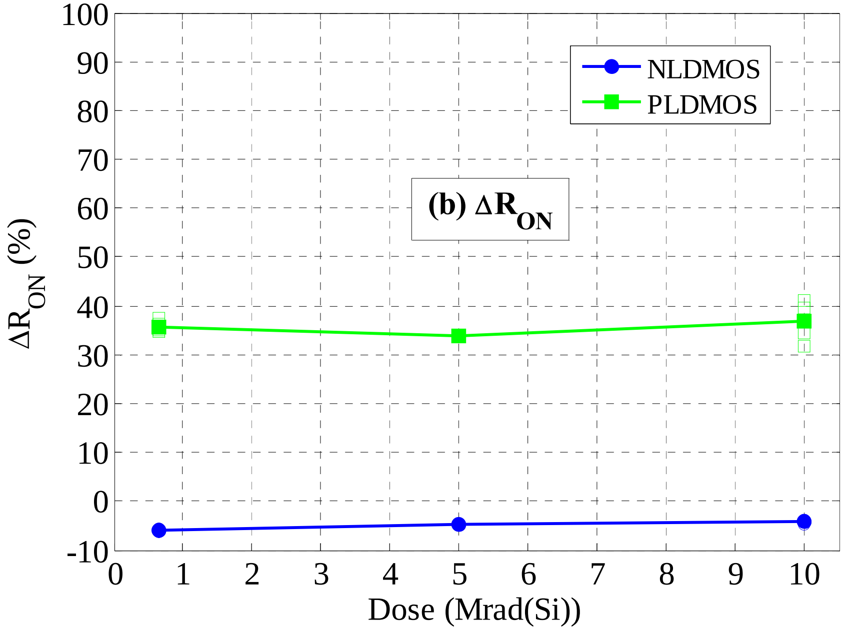
– Max ΔV_T ~ + 20 mV for NLDMOS devices
  - Quantitatively in accordance with ΔV_T observed after neutron irrads
  - “Rebound” not observed: probably interface traps dominant in this case

– Max $\Delta|V_T|$~+ 60 mV for PLDMOS devices
  - Same ΔV_T shift observed after neutron irrads

– V_T shifts observed after n irrads are mostly due to parasitic TID

Results (gamma irrads)

- **ΔR_{ON}** = $(R_{ONf} - R_{ON0}) / R_{ON0}$ (%)



  - Negligible changes of R_{ON} for NLDMOS
  - Little changes of R_{ON} (related to ΔV_T) for PLDMOS
  - R_{ON} change observed in neutron irrads induced by atomic displacement damage

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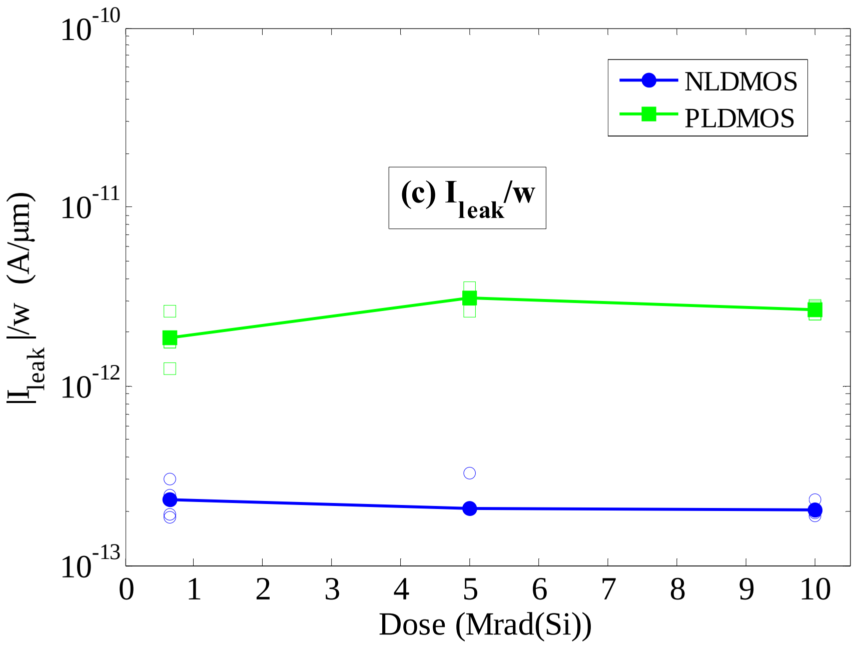
Results (gamma irrads)

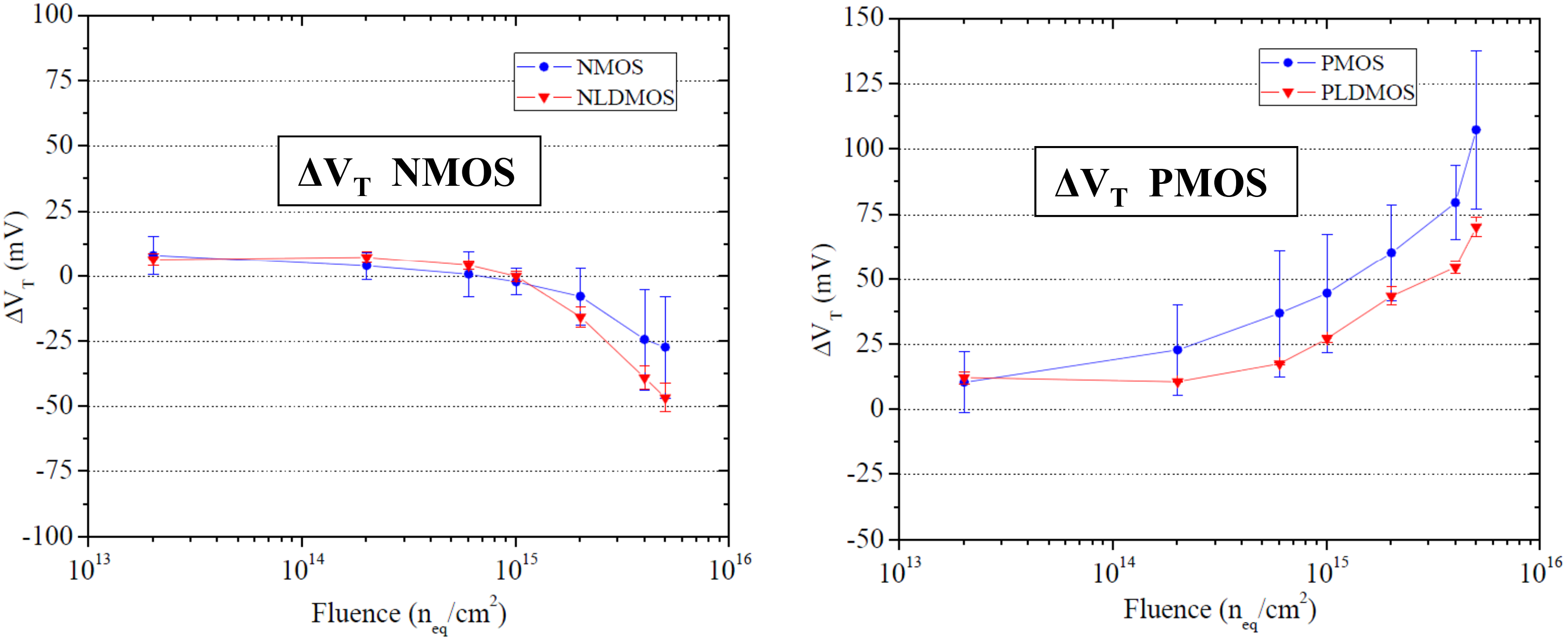
- I_{leak}/w



  - Negligible changes of I_{leak} for NLDMOS and PLDMOS
  - I_{leak} change observed in neutron irrads induced by atomic displacement damage

Standard MOS devices of IHP SGB25V tec

- Several standard MOS devices also present in the irradiation test chip
  - Very similar channel structure as LDMOS devices
  - Irradiated at the same neutron fluences, under the same conditions as the LDMOS devices



  - Very similar degradation of V_T as LDMOS devices
    - Confirms that V_T change in LDMOS is due to TID effects in the channel region

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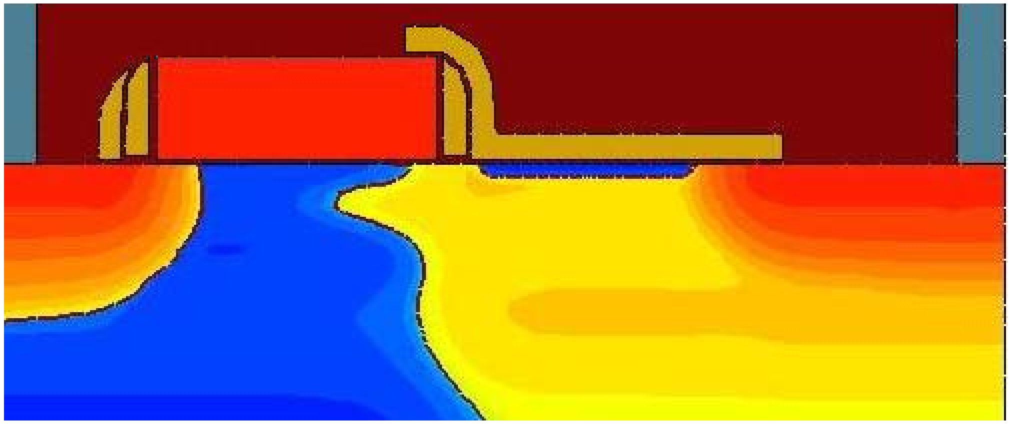
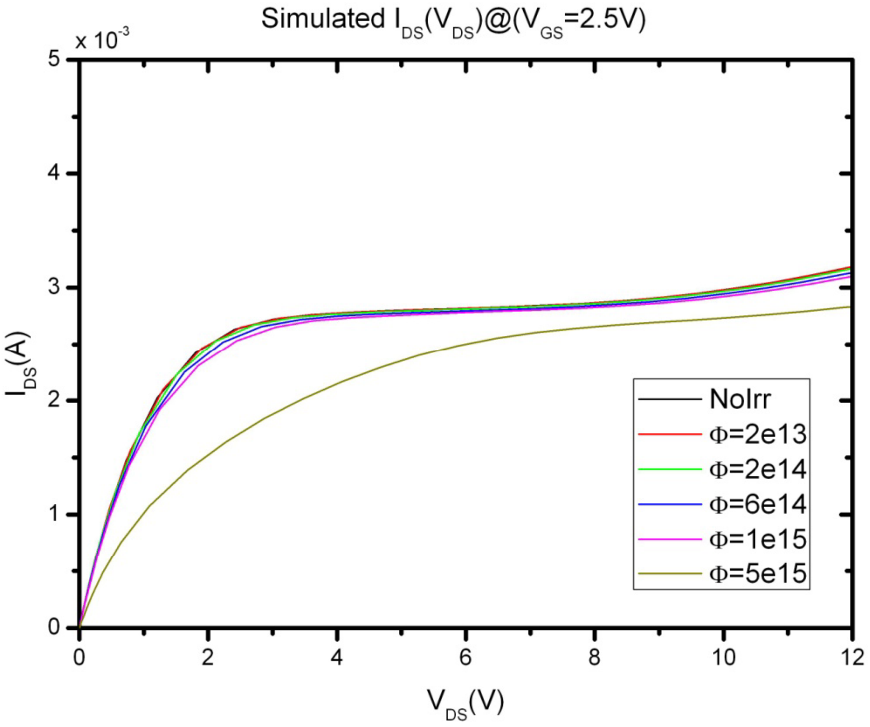
Simulations

- Technological and electrical simulations of IHP GOD LDMOS devices
- Status:
  - Pre-irrad electrical behavior reproduced (starting point)
  - Radiation damage mechanisms being implemented at the moment





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Conclusions

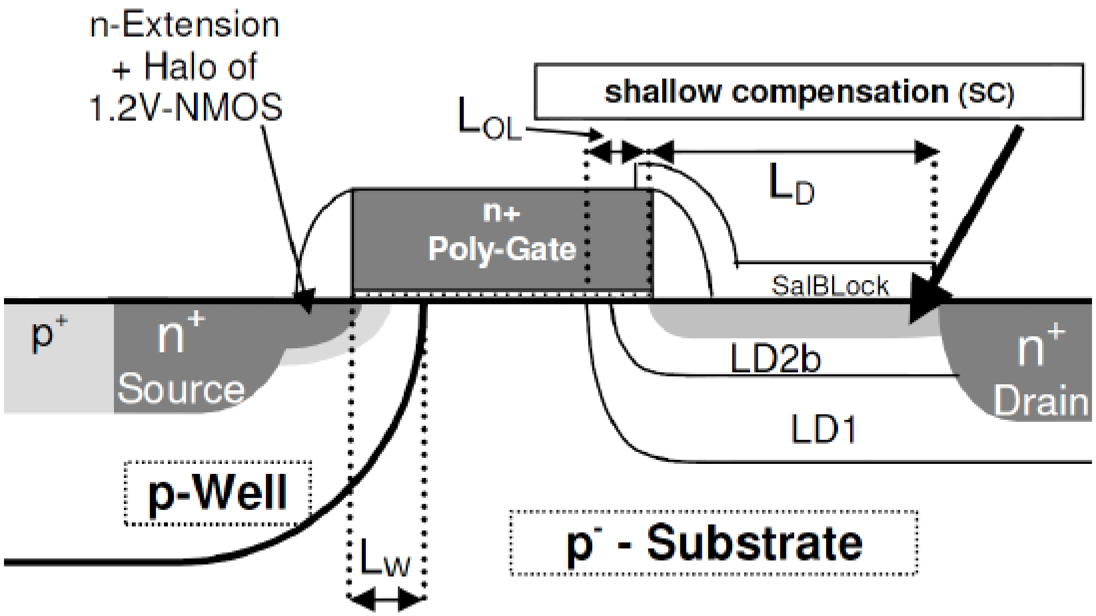
- Nonionizing radiation tolerance of 2nd generation SGB25V GOD LDMOS devices from IHP studied
- Degradation of electrical characteristics only observable at fluences equal or higher than $1\text{x}10^{15}$ n_{eq}/cm^2
- NLDMOS & PLDMOS devices exhibit small shifts of V_T and I_{leak} at the highest fluence ($5\text{x}10^{15}$ n_{eq}/cm^2)
- Moderate increase of R_{ON} for NLDMOS devices at $5\text{x}10^{15}$ n_{eq}/cm^2
- R_{ON} of PLDMOS devices increases dramatically at $5\text{x}10^{15}$ n_{eq}/cm^2
- On the whole, NLDMOS devices are suitable for its application in the SLHC from the p.o.v. of nonionizing radiation tolerance
- PLDMOS devices seem more “troubling”

Future work

- Ongoing simulations will help understand PLDMOS behavior and radiation damage mechanisms
- Understanding 3rd generation issues in collaboration with IHP and F. Faccio
- Study the new LDMOS technology generations from IHP
- SEB and SEGR studies

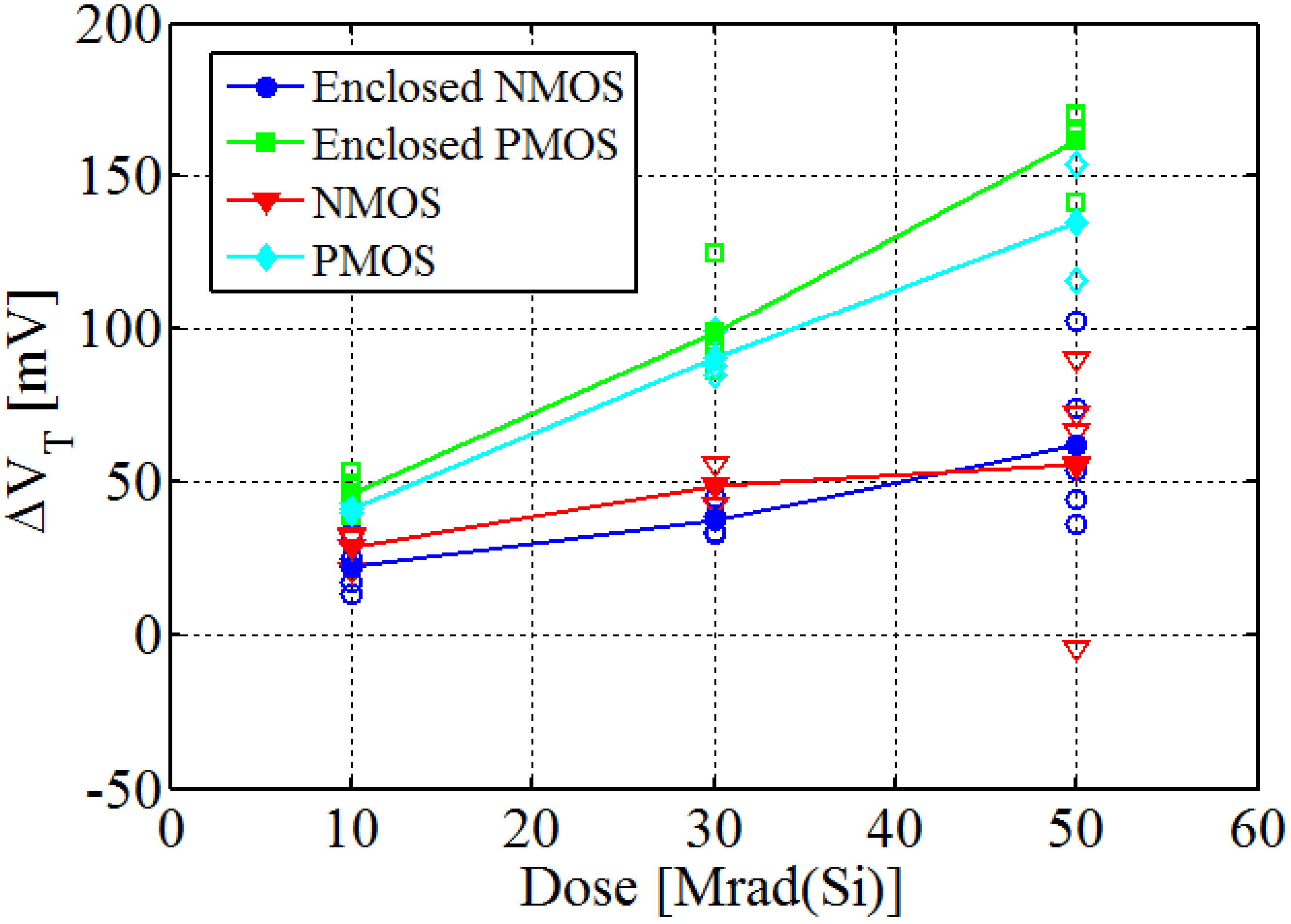
Thank you for your attention

NLDMOS detailed cross-section



Mohapatra et al., ESSDERC proc., 2005

Gamma irrads on standard MOS devices



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