Contribution ID: **56** Type: **Oral**

Radiation-hard power LDMOS devices for DC-DC conversion in the ATLAS Upgrade experiment

Thursday, September 23, 2010 12:15 PM (25 minutes)

This work presents radiation hardness studies performed on LDMOS devices of SGB25VGOD technology from IHP Microelectronics. These devices would constitute the power switches of the buck converters on the DC-to-DC powering scheme for the ATLAS Upgrade silicon tracker. Devices were irradiated with neutrons up to the target fluences expected inside ATLAS Upgrade. They exhibited very good radiation tolerance after irradiations, showing only minor increases of the threshold voltage and the on-resistance. These results make the devices suitable for their application in the silicon tracker. Additionally, simulations of the neutron irradiations were performed on technologically emulated LDMOS devices. Simulations reproduced quantitatively the on-resistance variations observed experimentally at the highest fluences.

Summary

The planned upgrade of the LHC experiment, the so-called Super-LHC (S-LHC), will increase the luminosity of the machine up to a instantaneous luminosity of L = 1e35 cm^(-2)s^(-1). The ten-fold increase in luminosity will lead to a ten times more severe radiation environment inside the detector, along with an increase on the multiplicity of particles created in each collision. In order to deal with the increased multiplicity, the inner tracker of the upgraded ATLAS detector has been designed with approximately 10x increased granularity. Due to material budget and power constraints, it has become critical an efficient, low-noise power distribution for the tracker on-detector readout ASICs. One of the proposed powering schemes for the ATLAS Upgrade silicon tracker stave modules is based on a two-stage DC-DC conversion. The conversion stage in the modules, proposed by the CERN Microelectronics group, would be performed by means of buck DC-DC converters. The main circuit units of these converters are the power switches, for which Laterally-Diffused MOS (LDMOS) devices are usually the best choice. LDMOS devices of SGB25V GOD technology from IHP Microelectronics [1] constitute the main technological option selected. Several prototypes have already been designed on this technology, with very promising results [2]. However, radiation tolerance of the IHP LDMOS devices is still an issue to be well understood in order to predict the electrical behavior of the circuit after the radiation levels expected inside ATLAS Upgrade.

In this work, we present results from several radiation hardness experiments performed on these type of devices, as well as electrical simulations of the radiation effects on the devices. Second-generation N and P LDMOS devices from IHP SGB25V GOD technology were irradiated at several neutron fluences, up to 5e15 neq/cm2. Irradiations were performed in the TRIGA nuclear reactor at Jozef Stefan Institute, Ljubljana. Results showed that the main effect of nonionizing radiation in the LDMOS devices was an increase of the on-resistance at very high fluences. Devices showed negligible radiation degradation (ΔVT < 50 mV, ΔRON < 10%, Ileak < 5 pA/μm) at fluences up to 1e15 neq/cm2. Devices irradiated at 5e15 neq/cm2 exhibited significant variations in the on-resistance parameter, showing increases of RON higher than 50% in comparison with the pre-irradiation values, along with slight changes on the threshold voltage, attributable to parasitic ionizing dose produced in the neutron irradiation facility. P-LDMOS devices revealed higher degradation in general than N-devices. Nevertheless, radiation tolerance exhibited by the devices makes them suitable for their application in the S-LHC.

In addition, Synopsys Sentaurus TCAD finite element simulations have been performed on technologically emulated LDMOS devices to predict their electrical behavior after the neutron irradiations performed. This tool proved to be very useful in order to understand the nonionizing radiation damage mechanisms on the devices. Simulations performed on the N-LDMOS devices reproduced quantitatively the RON variations observed at the highest fluence (ΔRON ~ 50% at 5e15 neq/cm2).

References:

[1] IHP Microelectronics: (http://ihp-microelectronics.com)

[2] S. Michelis et al. “Rad-Hard DC/DC Converters,” presented in ATLAS Upgrade Week, Hamburg, April 2010.

Primary authors: Dr ULLAN COMES, Miguel (Instituto de Microelectronica de Barcelona - Centro Nacional

de Microelectronica IMB-CNM (CSIC)); Mr DIEZ CORNELL, Sergio (Instituto de Microelectronica de Barcelona - Centro Nacional de Microelectronica IMB-CNM (CSIC))

Co-authors: Dr FLORES, David (Instituto de Microelectronica de Barcelona - Centro Nacional de Microelectronica IMB-CNM (CSIC)); Dr KNOLL, Dieter (IHP Microelectronics); Dr PELLEGRINI, Giulio (Instituto de Microelectronica de Barcelona - Centro Nacional de Microelectronica IMB-CNM (CSIC)); Dr CORTES, Ignacio (Instituto de Microelectronica de Barcelona - Centro Nacional de Microelectronica IMB-CNM (CSIC)); Dr LOZANO, Manuel (Instituto de Microelectronica de Barcelona - Centro Nacional de Microelectronica IMB-CNM (CSIC)); Mr FERNANDEZ-MARTINEZ, Pablo (Instituto de Microelectronica de Barcelona - Centro Nacional de Microelectronica IMB-CNM (CSIC)); Dr SORGE, Roland (IHP Microelectronics); Dr HIDALGO, Salvador (Instituto de Microelectronica de Barcelona - Centro Nacional de Microelectronica IMB-CNM (CSIC))

Presenter: Mr DIEZ CORNELL, Sergio (Instituto de Microelectronica de Barcelona - Centro Nacional de Microelectronica IMB-CNM (CSIC))

Session Classification: Radiation tolerant components and systems

Track Classification: Radiation tolerant components and systems