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A readout driver for the ATLAS LAr calorimeter at super-LHC

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A new readout driver (ROD) is being developed as a central part of the signal processing of the ATLAS liquid-argon calorimeters for operation at the sLHC. In the architecture of the upgraded readout system, the ROD modules will have several challenging tasks: receiving of up to 1.4 Tb/s of data per board from the detector front-end on multiple high-speed serial links, low-latency data processing, data buffering, and data transmission to the ATLAS trigger and DAQ systems. In order to evaluate the different components, prototype boards in ATCA format equipped with modern Xilinx and Altera FPGAs have been built. We will report on the measured performance of the SERDES devices, the parallel signal processing using DSP slices, the implementation of trigger interfaces, using e.g. multi-Gb Ethernet, as well as the development of the ATCA infrastructure on the ROD prototype modules.

Summary

The ATLAS experiment is one of the two general purpose detectors designed to study the proton-proton collisions at the Large Hardron Collider (LHC). The liquid-argon (LAr) calorimeters of ATLAS are measuring energy deposits of electromagnetic particles and to trigger on interesting physics events. The readout and trigger electronics of the LAr calorimeters amplify, shape, digitize and process the signals of in total 182,486 detector cells. The current front-end and back-end electronics are planned to be replaced in order to cope with the even more challenging experimental environment at a future upgraded super-LHC (sLHC) collider. Several reasons imply the installation of a new-generation readout: higher radiation levels for the on-detector electronics and thus total ionization dose levels beyond those for which the current electronics is qualified, more simultaneous proton-proton interactions and pile-up background, natural ageing of the current electronics, and the limited size of on-detector data buffers which prevent other detector and trigger systems to implement more advanced trigger processing which eventually leads to longer latency times of the trigger accept signals.

In the new readout architecture that is currently being developed, the readout drivers (ROD) will play a central role. The ROD modules are supposed to receive digitized data from all front-end channels, with effective 16 bit precision per channel and at the full bunch crossing frequency of 40 MHz. The geometrical arrangement of the detector cells and the trigger layout suggest that data from groups of 14 front-end boards (FEB), each covering 128 channels, are processed by one new ROD. The data of each board is planned to be transmitted by high speed optical links, running at 10 Gb/s per fiber which are combined to ribbons with 100 Gb/s per FEB. The input data rate is therefore about 1.4 Tb/s per ROD. To handle this large amount of data, parallel processing in high performance FPGA devices is foreseen. ROD prototype boards in ATCA format with Xilinx Virtex-5/6 and ALTERA Stratix II/IV are being used to evaluate the SERDES components. Single fiber links at up to 6.25 Gb/s were run successfully and transmission of 12 x 6.25 Gb/s on ribbons is being worked on, as well as going towards faster individual link speed.

After deserialization, there are multiple tasks that the ROD has to perform. From the digitized data, energy, time and quality of the signal pulse are extracted by using an FIR filter. After bunch-crossing identification, the trigger information is calculated and sent to the trigger processors via additional optical links. The latency requirements of the very first trigger level (level-0) put stringent limits on the time budget which must stay below ~450 ns. Also the data flow to the trigger is non negligible with approximately 256 Gb/s and 13 Gb/s to the planned level-0 and level-1 trigger processors, respectively. These tasks are being implemented individually into FPGA on ROD prototypes to evaluate the algorithmic performance. Also the data buffering concepts for the trigger levels are being tested. Eventually, after receiving the trigger accept signal, data is transmitted to the buffer system for the higher trigger levels. Here,10 Gb/s Ethernet on FPGA is being implemented in order to allow the usage of commercial PC or ATCA components for buffering and communication with the subsequent DAQ stages.

In the presentation, an overview about the various components necessary to develop this new and complex ROD system will be given. The current R&D activities and architectural studies of the LAr Calorimeter group will be presented, in particular the on-going design of the high-speed off-detector FPGA based processing units, results on fast signal processing, as well as on the development of interfaces to the different trigger pro-

cessing devices. The experience of system development within the ATCA environment will also be reported on.

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