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ATLAS IBL: Integration of new hw/sw readout features for the additional layer of pixels

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An additional inner layer for the existing ATLAS pixel detector, called insertable B-layer (IBL), is under design and it will be installed by LHC-PHASE1. New front-end readout ASICs have already been fabricated and will replace the previous chips in this layer. The new system features higher readout speed - 160Mbit/s per ASIC - and simplified control. The current data acquisition chains are composed of front-end detectors, readout chips, back-of-crate (BOCs) cards and readout driver cards (RODs). The paper presents a proposal for the new ROD board, which implements modern FPGAs and high-speed links with the detector and with the ATLAS DAQ system.

Summary

The new ATLAS insertable B-layer (IBL) readout system will carry out the same functions implemented in the current back-of-crate (BOC) and readout driver (ROD) cards. The new IBL B-layer features electronics DAQ boards with modern and powerful programmable devices and high-speed links. Except the new IBL system, the current readout architecture that is implemented in ATLAS pixel layers 1 and 2 and in all layers of SCT strips will be maintained unchanged. Particularly, the current system interfaces the front end at a rate that ranges from 40 to 160Mbit/s, depending on the layer and on the type of detector. At maximum rate in the B-layer, one BOC-ROD pair currently interfaces 8 modules – 16 front-end ICs (FE-I3) - at 160Mb/s and the data throughput is balanced for 1 S-Link on the BOC card at 1Gbit/s. Conversely, the aim of the new ROD card under design and development for IBL is to interface with 32 FE-I4 ASICs at a rate of 160 Mbit/s and with the ATLAS DAQ system using 4 S-Links. Moreover, a novel approach to carry out histograms and analysis is proposed by transferring data to a pc-farm via fast Gbit/s Ethernet links. These features allow for executing calibration and fits off-line instead of using DSP components on the ROD card as it is done now. Also the total calibration processing time will be reduced. In more detail, the new ROD will execute only the calibration loops to accumulate the sums of threshold, time-over-threshold and time-over-threshold-squared parameters. Then histograms are created and saved on-the-fly on RAMs and eventually transferred via Gbit/s Ethernet to an off-line high-performance computer. The new ROD card – see figure - proposes two XILINX Spartan6 programmable devices and one Virtex5 with Power PC capabilities. These commercial devices permit also to reuse most of the VHDL code that has been designed to implement the firmware on the current ROD card for the ATLAS pixel and SCT experiments. The new BOC-ROD system prototype is foreseen by early 2011 and is going to be tested on the same 64x VME-based crates that are now implemented for the ATLAS pixel and SCT DAQ detector. The new IBL system is scheduled to be mounted in the LHC-PHASE1.

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