

SPACIROC

Spatial Photomultiplier Array Counting and Integrating ReadOut Chip

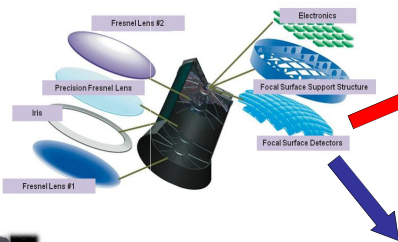
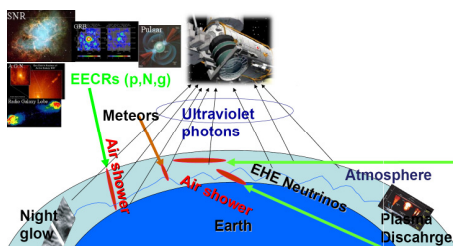
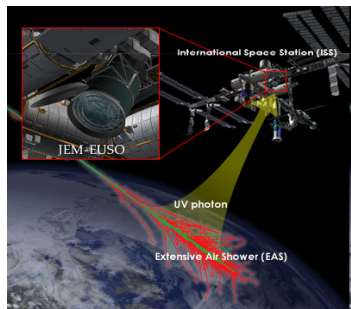
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Description

- Readout chip for 64 channels MAPMT
- Front End ASIC for JEM-EUSO mission
- Low-power (1mW/ch) & radiation hardened for space application
- Co-designed by LAL/JAXA/RIKEN

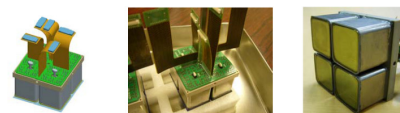
JEM-EUSO

- Extreme Universe Space Observatory on Japanese Experimental Module
- Extremely High Energy Cosmic Ray (EECR ~ 10^{20} eV) observer onboard of International Space Station
- Observing extensive air shower created by the EECRs
- Consortium of 12 countries led by Riken, Japan
- Currently in preparation for Phase B studies

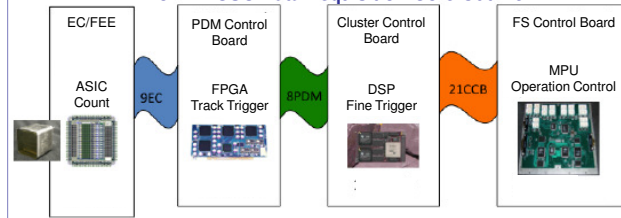


Focal Surface detectors:

- ~5000 MAPMTs (~300k pixels)
- Front End (FE) ASIC: SPACIROC
- Elementary Cell (EC): 4xSPACIROC + 4xMAPMT



JEM-EUSO Data Acquisition Core Outline

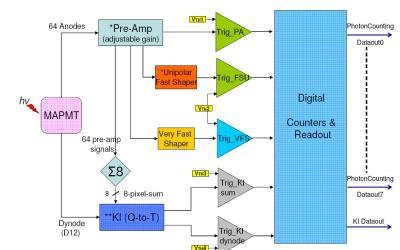


Specifications

- Single Photon Counting: 64 channels
 - 100% trigger efficiency > 1/3 photoelectron (pe)
 - Trigger pulse width < 10 ns
- TOT (Q-to-T): 1 channel for last dynode and 8 internal channels (summed signals)
 - Input range 15pe - 1500pe
- Consumption < 1mW/channel
- Gate Time Unit (GTU): 2.5µs
- 9 serial data output, 576-bit/GTU

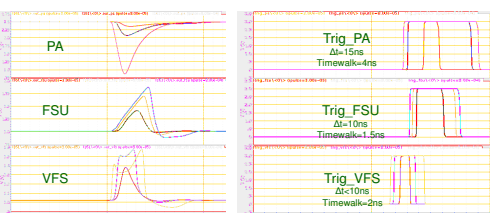
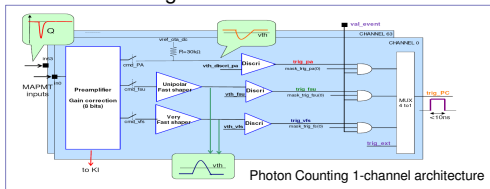
Architecture

- 64 adjustable gain MAPMT anodes Preamps
- 3 selectable triggers for Photon Counting:
 - Directly from Preamp signals (PA)
 - Unipolar Fast Shaper (FSU) – Adjustable gain
 - Very Fast Shaper (VFS) – Fixed Gain
- Photon Counting trigger width < 10 ns
- Time Over Threshold (Charge to Time conversion)/ KI based on KI02/03 chip (Japan)
 - Inputs:
 - MAPMT last dynode (1 channel)
 - Sum of 8 successive Preamp signals => 8-pixel-sum (8 channels)
 - Variable Trigger pulse width
- Digital: Counter for Photon Counting & KI, Data Transmission



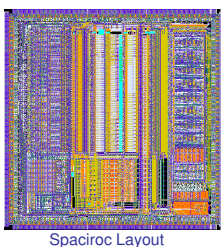
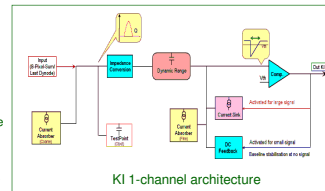
Photon counting - 1 channel

- 8-bit variable gain MAPMT preamp
- 3 triggers – selectable via Slow Control
- 10-bit dac for threshold
- Multiplexer to select internal or external triggers
- Channel masking



KI - 1 channel

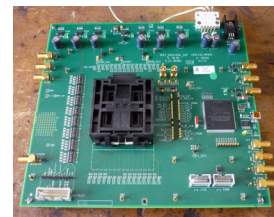
- Inputs: Last dynode, 8-pixel-sum
- Tunable dynamic range for charge integration
- Adjustable charge integration duration (4-bit Slow Control)
- Channel masking, External trigger select



Spaciroc Layout

Chip status:

- Received in October 2010
- Process: AMS 0.35µm SiGe
- Dimensions: 4.6mm x 4.1mm (19 mm²)
- Power supply: 0-3V
- Packaging: CQFP240 (proto) FPBGA144 (EC board)



Spaciroc Test Board