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SPACIROC: Rad-Hard Front-End Readout chip for the JEM-EUSO telescope

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SPACIROC is designed for the JEM-EUSO observatory onboard of the International Space Station (ISS). This 64 channels readout ASIC offers photon counting capability and includes a charge to time (Q-to-T) converter. The main requirement for the photon counting is to obtain a 100% trigger efficiency starting from 1/3 p.e. with a 10 ns double pulse resolution. As for the Q-to-T converter, the chip needs to deliver a linear measurement for the input charges ranging from 10 p.e. to 300 p.e. Moreover, the ASIC was designed to achieve low power consumption (1mW/channel) and radiation tolerance, in compliance with the operating constraints imposed by the ISS. The current design of the ASIC was done in collaboration with RIKEN, Japan on behalf of the JEM-EUSO consortium. A prototype chip has been submitted for fabrication in March 2010 using AMS SiGe 0.35µm process.

Summary

The primary purpose of JEM-EUSO experiment is to detect the Extreme Energy Cosmic Rays (EECR).
Such high energetic particles will produce fluorescence signal when they pass through the atmosphere. By observing the phenomena from the International Space Station, this telescope will be able to identify the EECR.
Multi-anode photomultipliers (MAPMT) are proposed to equip the telescope's focal surface. SPACIROC was designed specifically to accommodate the readout of these MAPMTs. For this mission, the ASIC is required to count detected photons and to perform charge to time (Q-to-T) conversion. SPACIROC offers 64 inputs dedicated to the anodes of one MAPMT and 1 input for the last dynode. The specifications for the chip are the following:
- Photon Counting : 64 channels
- Q-to-T converter : 1 channel for last dynode + 8 internal channels (summed signal)
- 100% trigger efficiency for charge greater than 1/3 photoelectron (p.e.) with 10 ns double pulse resolution
- Q-to-T converter input range: 10 p.e. - 300 p.e
- Power consumption : 1 mW/channel
- 9 data serial outputs

For the photon counting, the preamplifier, the shapers and the discriminators are largely inherited from the MAROC3 chip. The input signal passes through a low-noise and low input impedance preamplifier with an individual variable gain. Afterwards, the amplified signal could be fed through shapers or into the Q-to-T converter. Currently, the chip offers 3 different triggers for photon counting. Depending on the shaper and discriminator selected, the chip could provide single p.e trigger pulse width smaller than 10 ns. To count the detected photons, a digital module was built for each channel around an 8-bit counter which could operate up to 100 MHz. At the end of each acquisition window (GTU), the counter values are readout through 8 serial links in order to reduce overhead.

As mentioned earlier, the first 8 inputs of the Q-to-T converter will take the pre-amplified signals from the photon counting (sum of every 8 channels). However, the 9th input takes a signal coming directly from the last dynode of the MAPMT. An impedance converter and a charge amplifier are used to transform the input signal into a voltage signal. Later, a trigger pulse is obtained by comparing the voltage pulse to an adjustable reference value. Adjusting this pulse width is easy: it is done via a variable gain current source. Finally, this trigger pulse will enable a digital counter. In a similar manner to the photon counting readout, the counter data are sent through a serial link at the end of each GTU. This converter was designed in collaboration with RIKEN, Japan. The design is based on their KI02 chip.

Several precautions have been taken into account during the design of SPACIROC to make sure it could operate in extreme conditions. For instance the layout was done carefully in order to minimize the Single Event Latchup effect. A mechanism to detect Single Event Upset was also added. Concerning the consumption, the ASIC should not exceed 1mW per channel. The design was done using AMS SiGe 0.35µm process. The final chip dimensions are 4.6 mm x 4.1 mm (19 mm^2). The ASIC was submitted for fabrication in March 2010.

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