Serial Power Protection for Atlas Strip Staves

- Introduction
- Discrete Circuit
- System Test Results
- Initial Approach on a Radiation Hard ASIC Implementation

J. Kierstead,P. Kuczweski, D. Lynn (BNL)
C. Musso (NYU)

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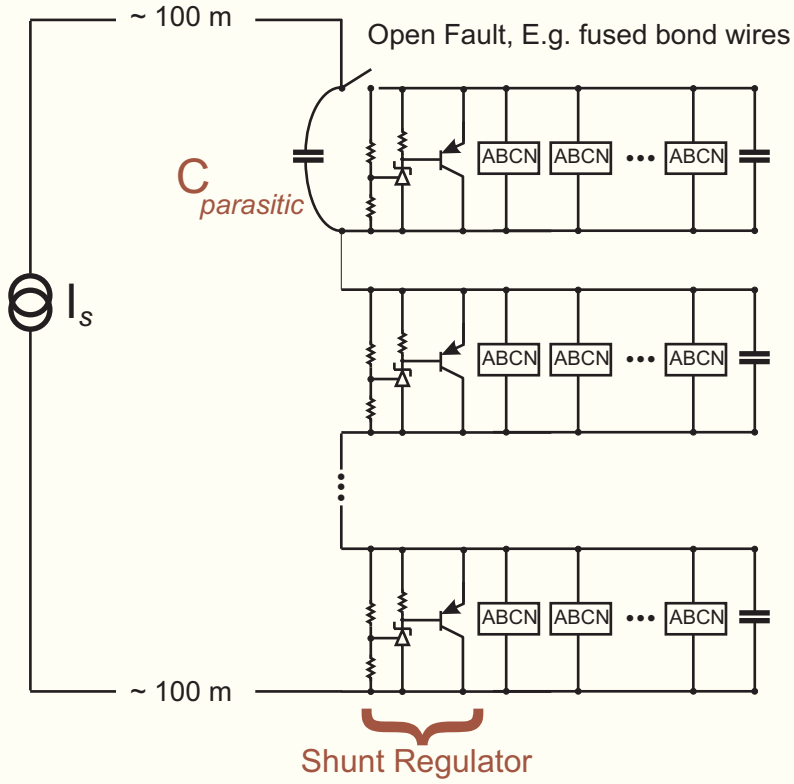
Motivation and Design of Serial Power Protection

- For a sudden open circuit, local protection is needed as current source power supplies are too far away to shut off current to stave; For example...

- If the current source is far away (~100m in Atlas), the quickest time current could be shut off at stave is approximately 200m / (2/3 speed of light) = 1μs.

- If I_s= 1 A , $\Delta V = \Delta t\ (I/C_{para})$ = 100kV!! Sparks would likely develop before the supply could respond and may unpredictably further damage stave and make a subsequent DCS enabled bypass ineffective. Stave may become inoperable.

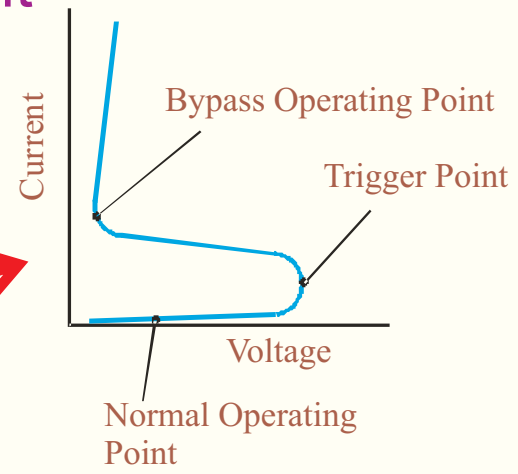


- In addition to such local *Real-Time* protection, a DCS (or slow controlled) enabled bypass is desirable, e.g. to short a noisy module, or short a module that draws too much current after irradiation. *Slow Control Bypass saves serial power chain from any non-real-time failure mode.*

Power Protection Board(PPB) Circuit

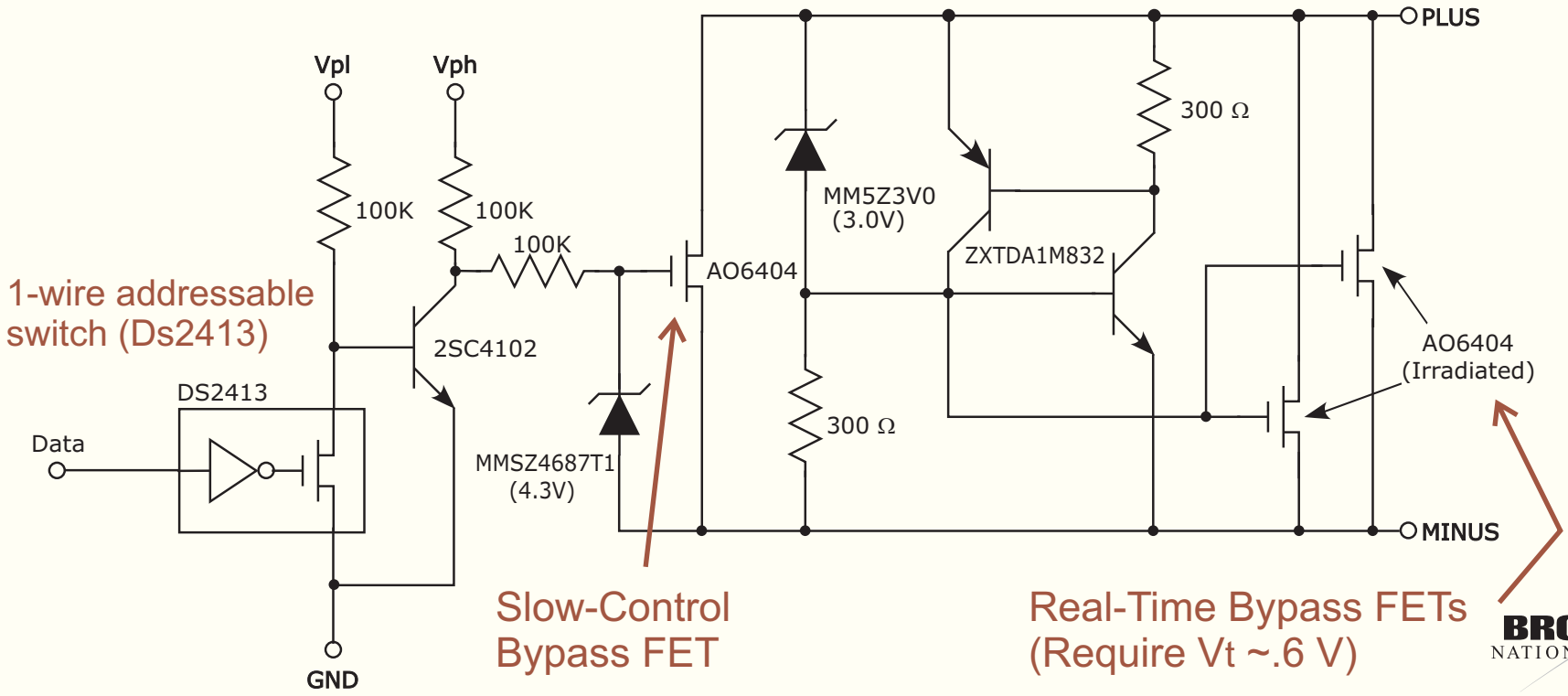
- Real-time circuit detects over-voltatge condition and latches Vds to less than 800 mV.
- DCS (or Maxim 1-Wire) enables user to short Vds to < 100 mV.

Note: Extra transistor 2SC4102 and pullup voltage are needed by 1-wire bypass because drain of output FET of the 1-wire device Ds2413 is rated only to 28 volts. Vph needs to be ~70V for 24 hybrids in series. Custom design would eliminate one transistor and pullup voltage.



DCS Enabled Bypass
(V_{ds} < 100 mV)

Real-Time Bypass
(V_{ds} < 800 mV)



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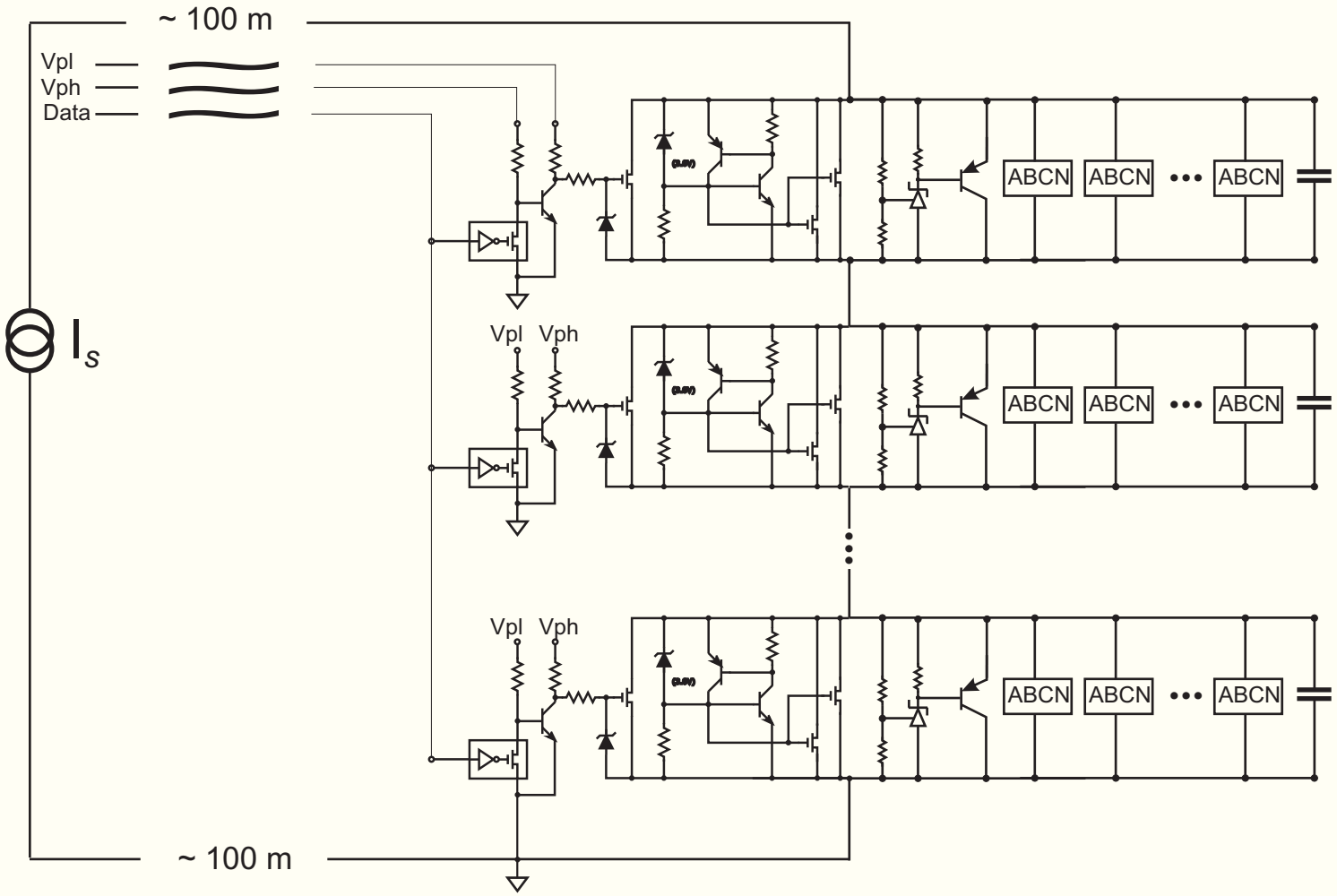
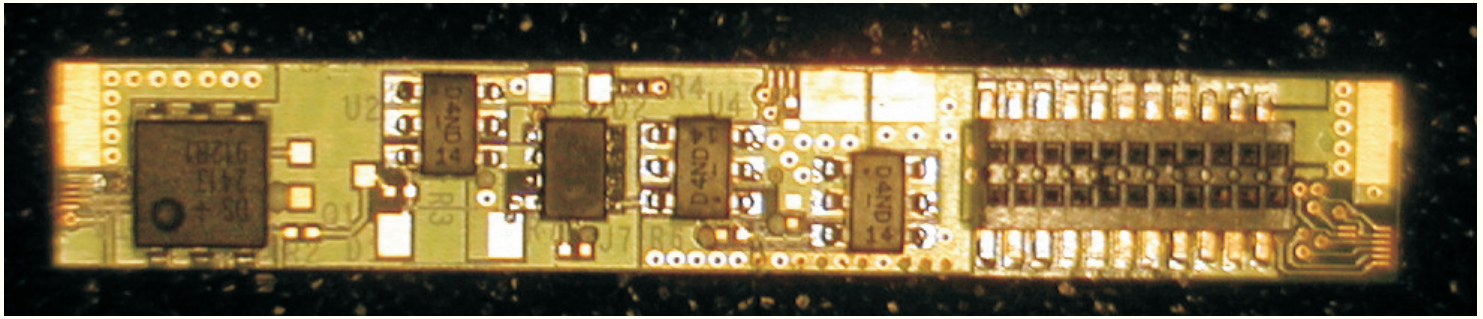
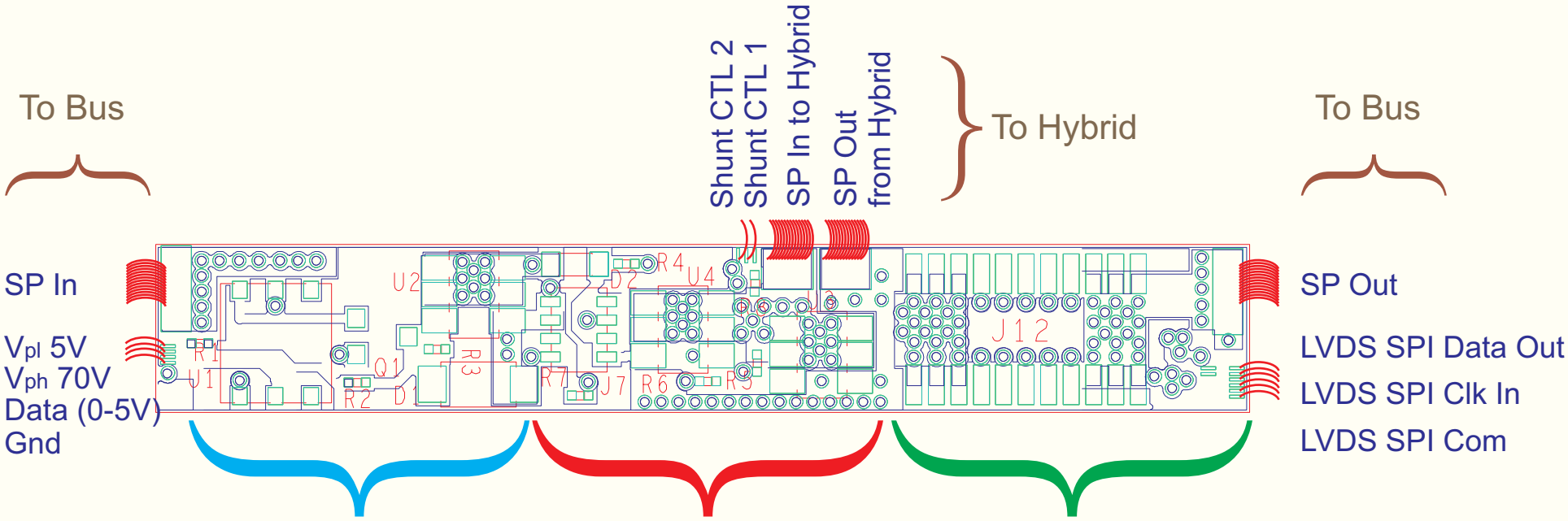
Stave I/O for 1-wire Bypass and System Architecture

- In current implementation four conductors for slow control bypass is needed for full serial power chain (Vpl, Vph, Data, Gnd)
- Could be reduced to two in custom implementation



Power Protection Board Layout





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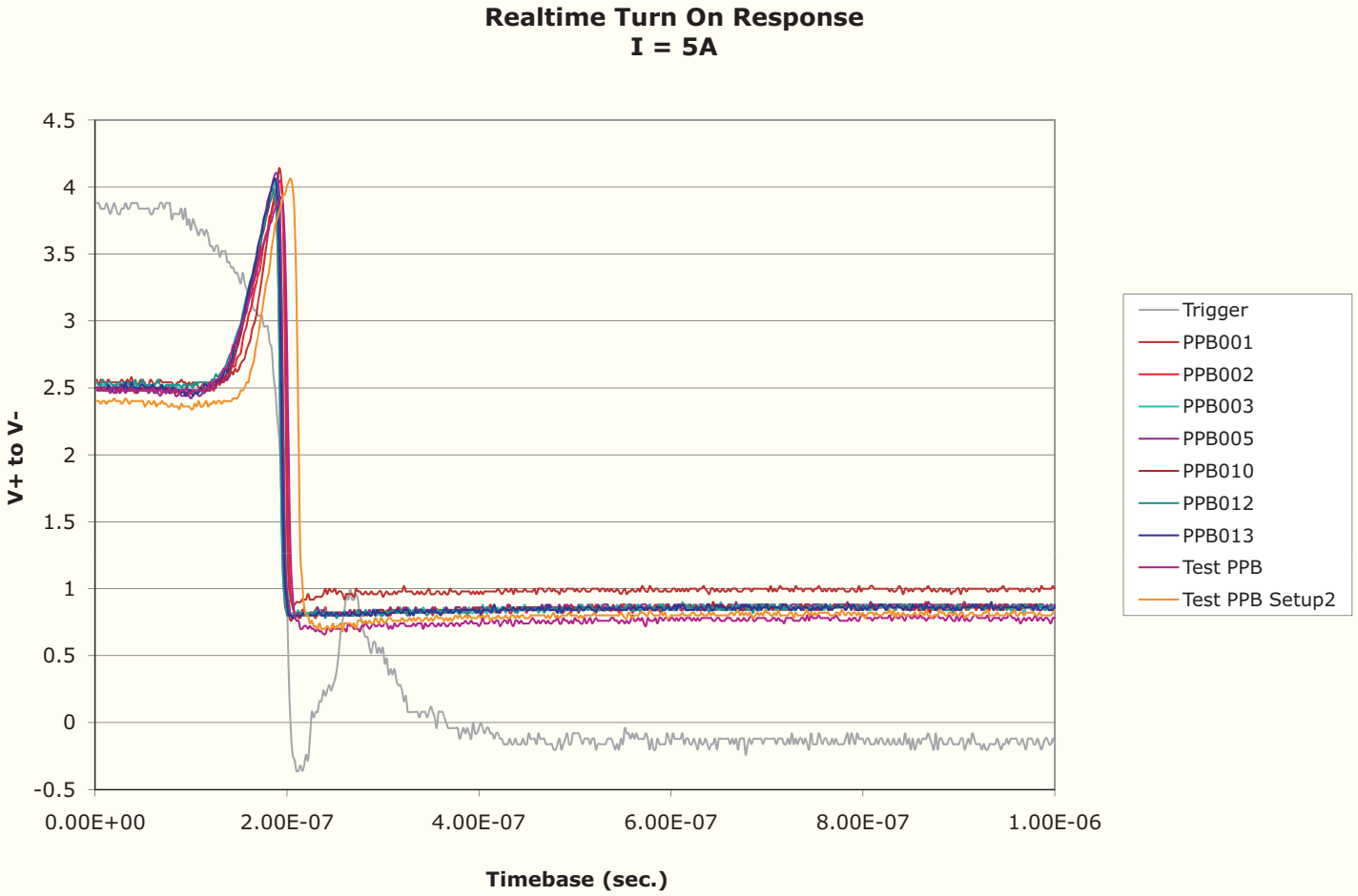
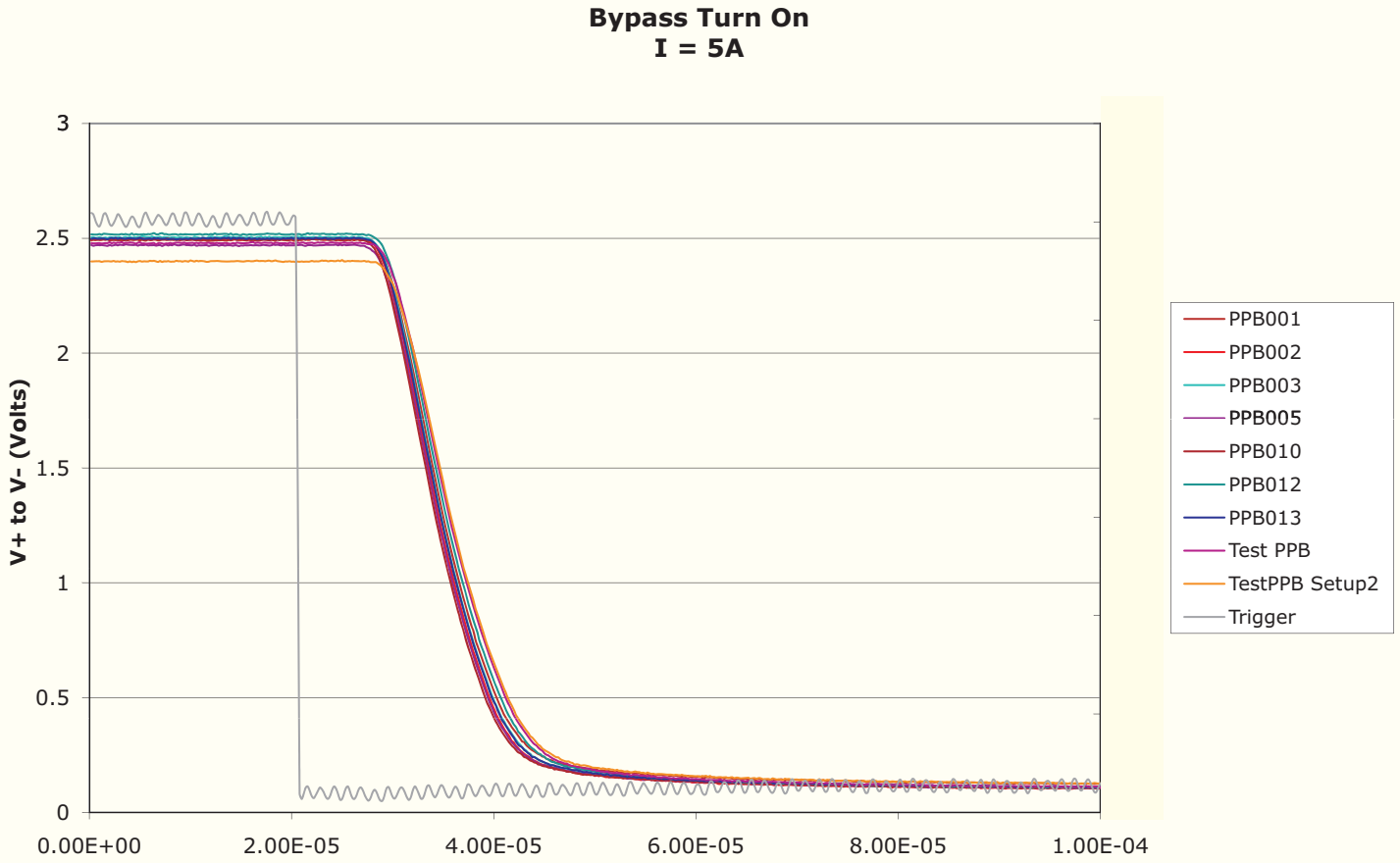
Uniformity of Real-Time Response

- Response of first eight circuits is pretty uniform
- Except for very first circuit (settles to ~ 1 volt), all other circuits settle to 0.7 to 0.8 volts



Uniformity of Bypass Enable Response

- Response of first eight circuits is pretty uniform
- Rail to rail voltages settle to about 100 mV



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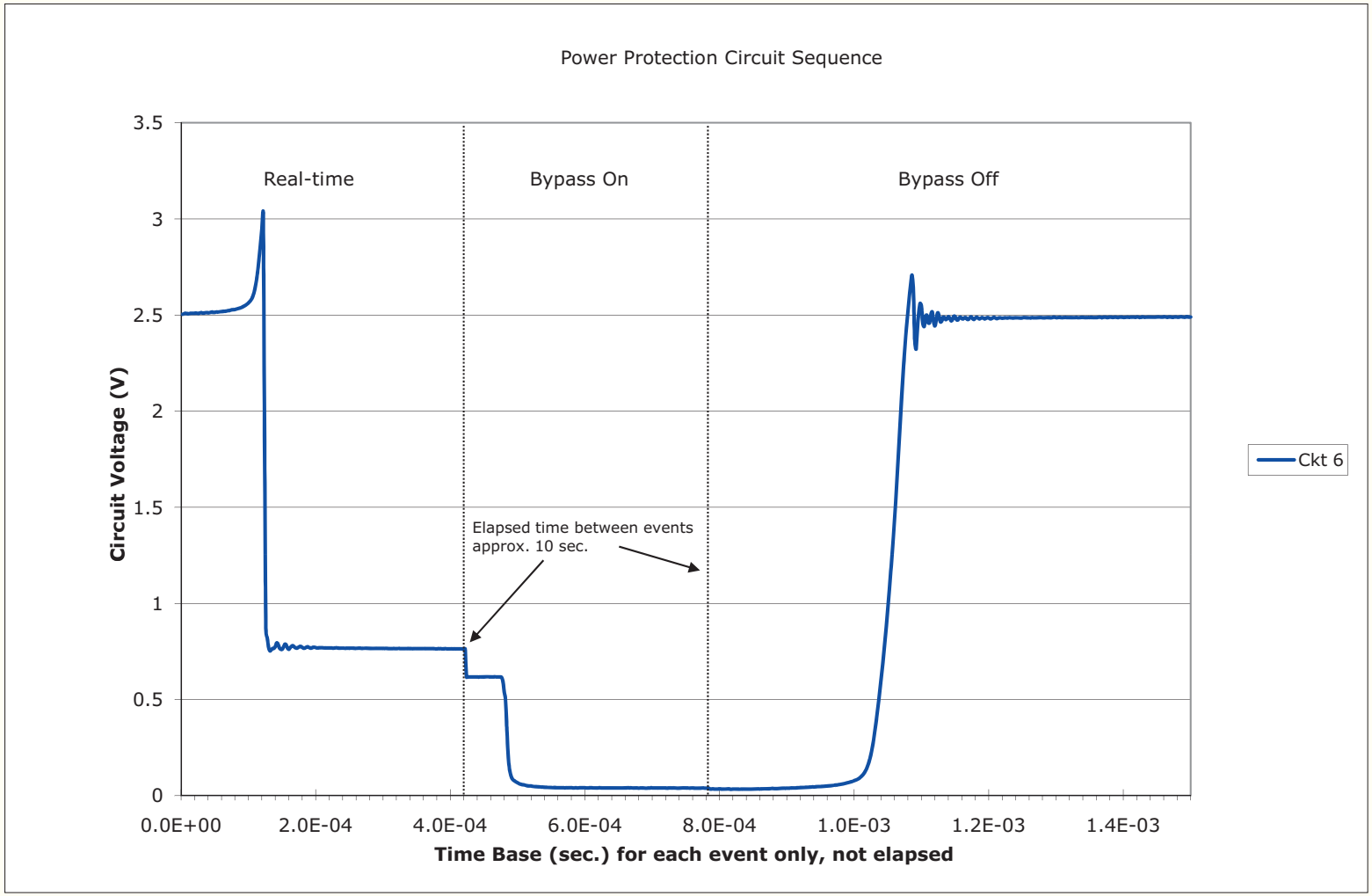
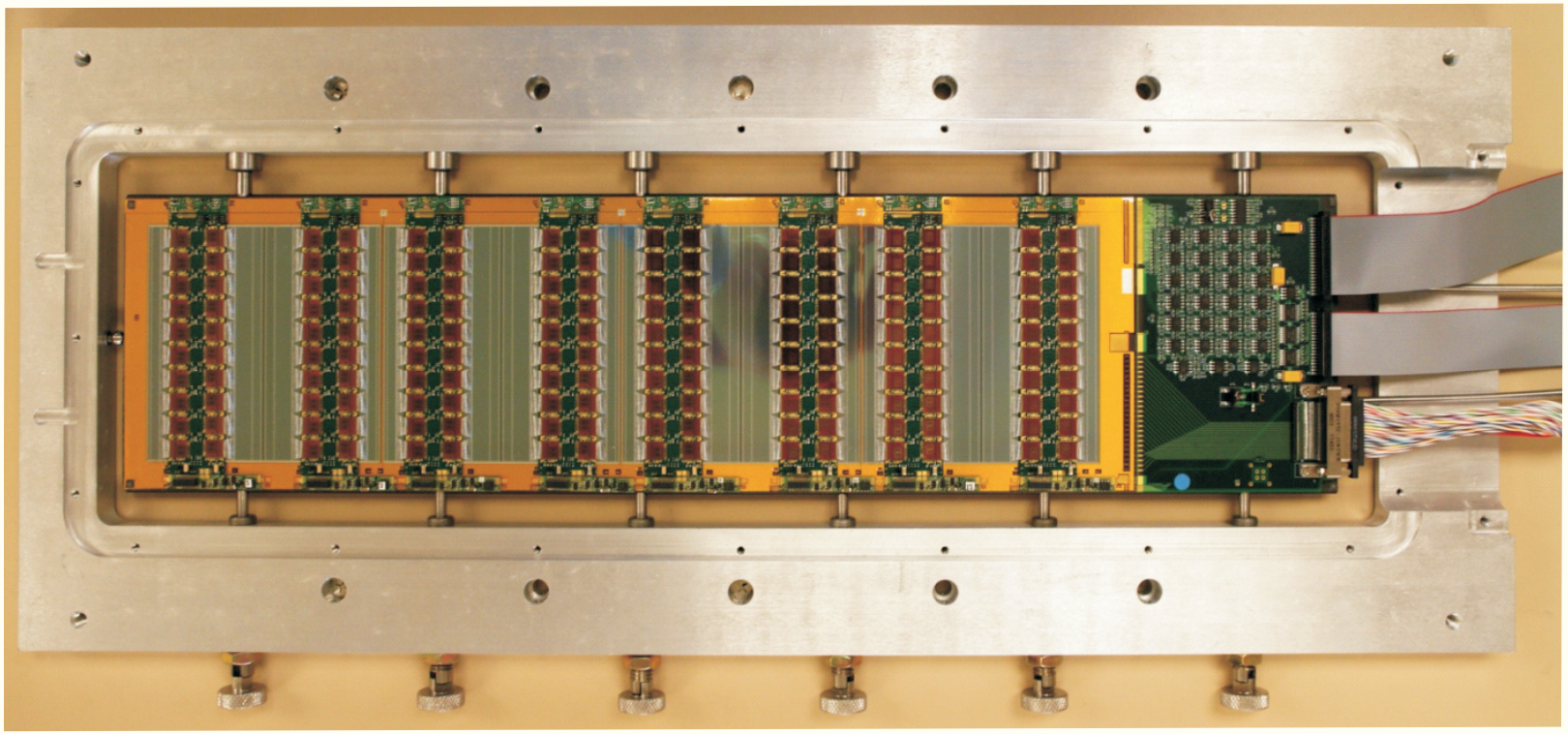
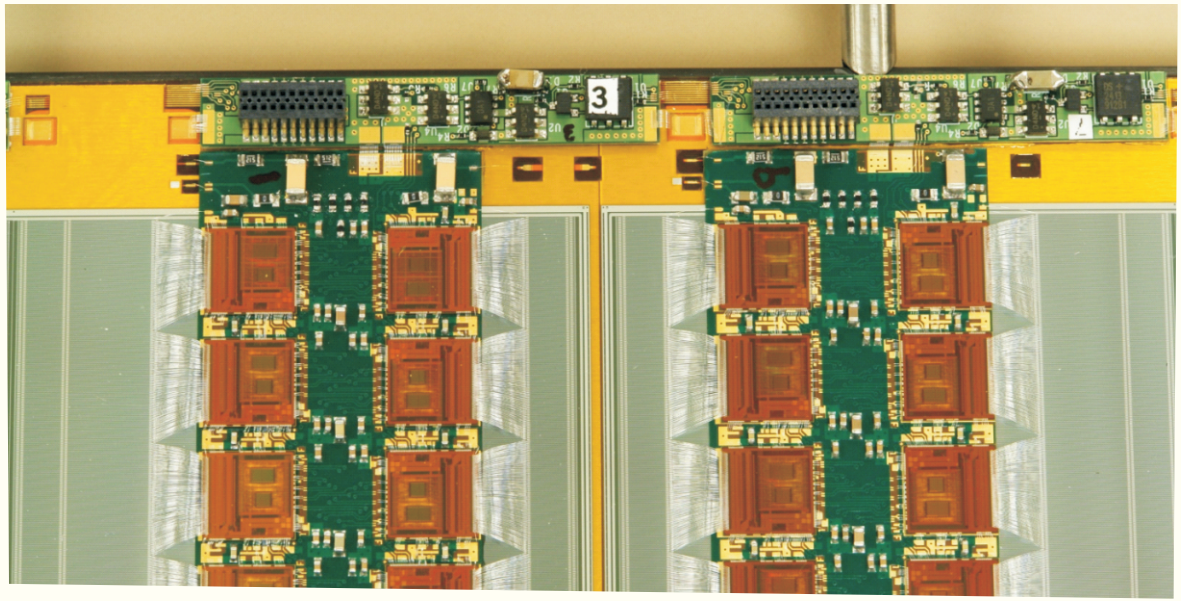
Resetting RT-Latch via Slow Control Bypass



Power Protection Board on First Stavelet

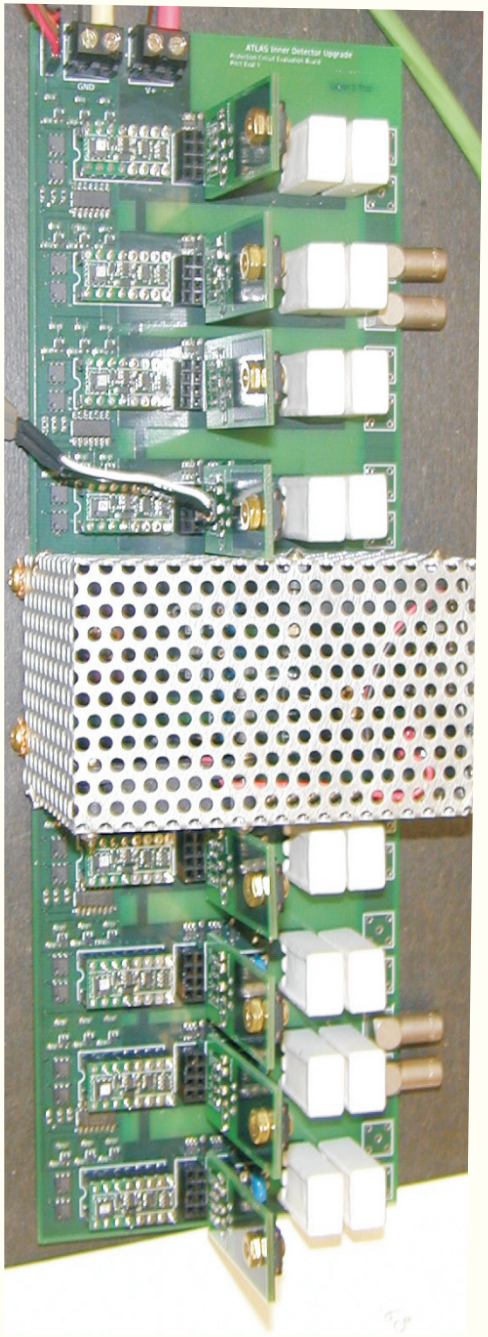


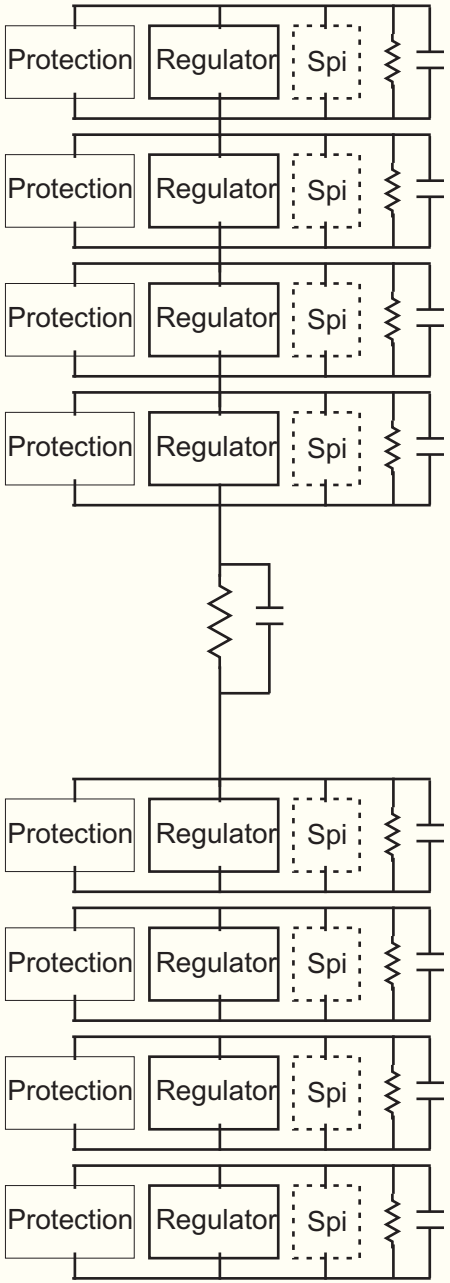


– It is expected that an ASIC implementation would be located on the hybrid

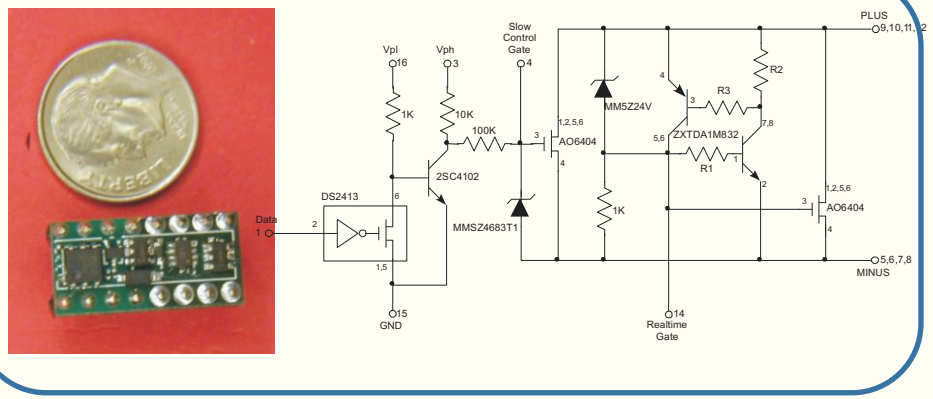
System Test Studies

SP System Test Board

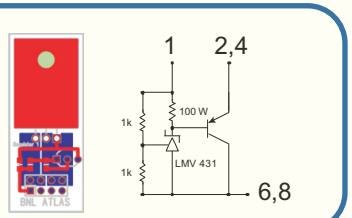




Protection Circuit- Protoype I



Regulator Board



SPi Board

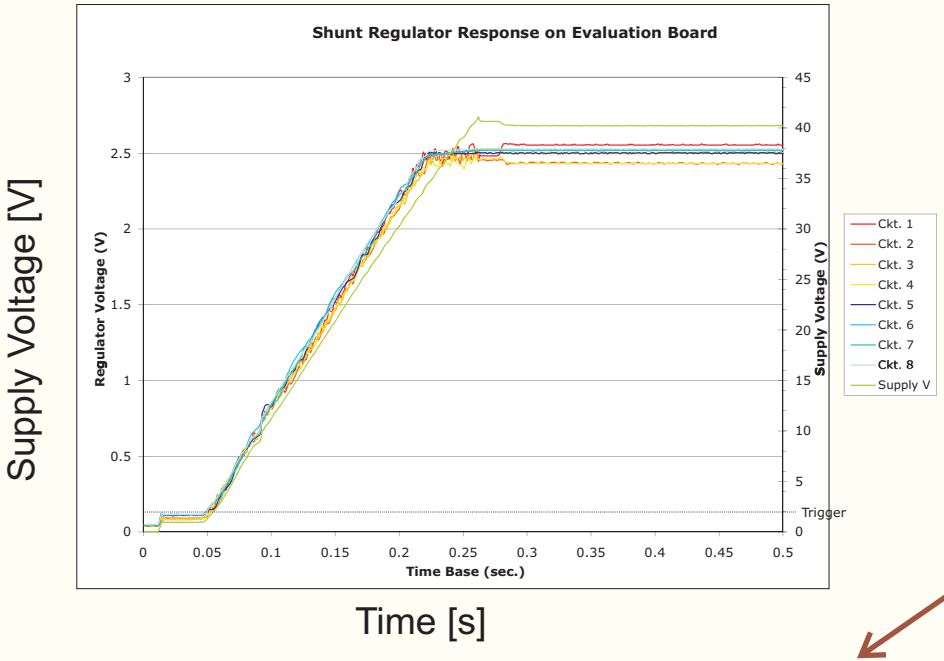
System Test Board

- Mimics 8 hybrids + 8 virtual hybrids
- 16 x 2.5 V = 40 volt operation
- Test real-time circuits; allows 1-wire controlled “open circuits” in variety of “hybrid” locations
- Test multiple 1-wire bypass circuits
- Mimics clock dependent variable module current loads for noise tests
- SPi chip compatible
- Study power-up issues

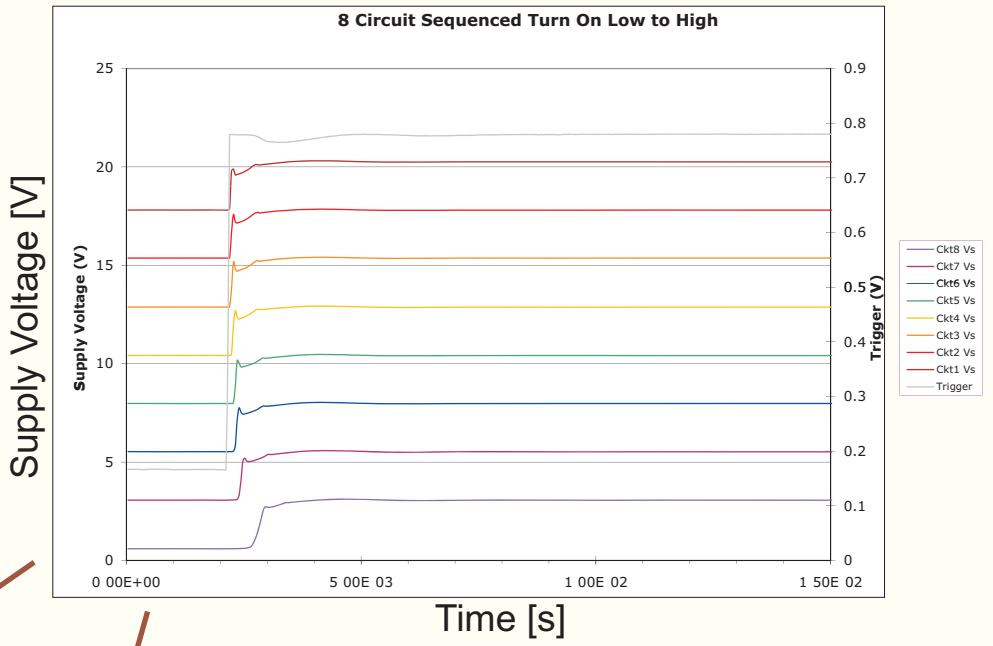
Note: Thermal issues limit current to 2.5 Amps

Simultaneous and Slow Control Power-Up of SP Chain

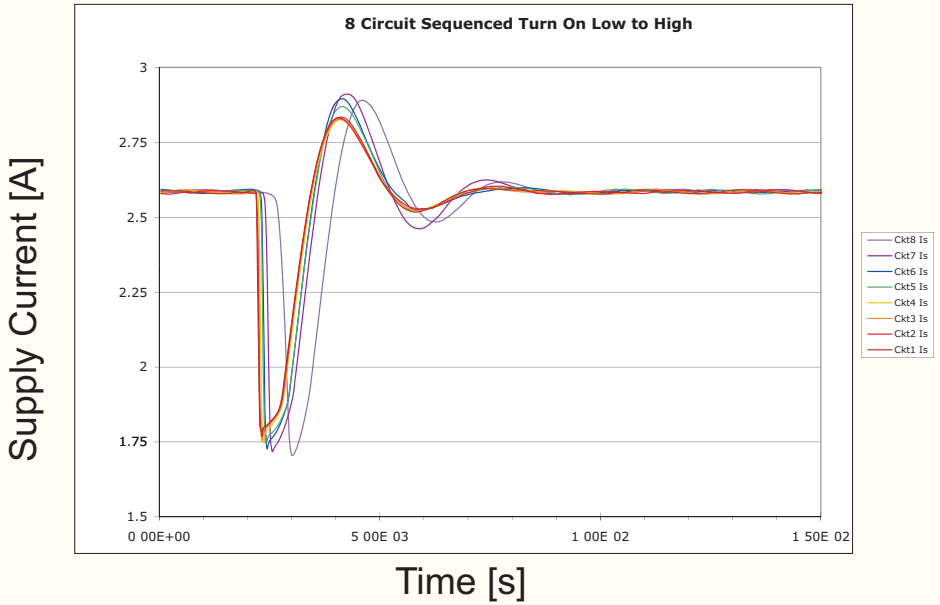
Simultaneous Power-Up



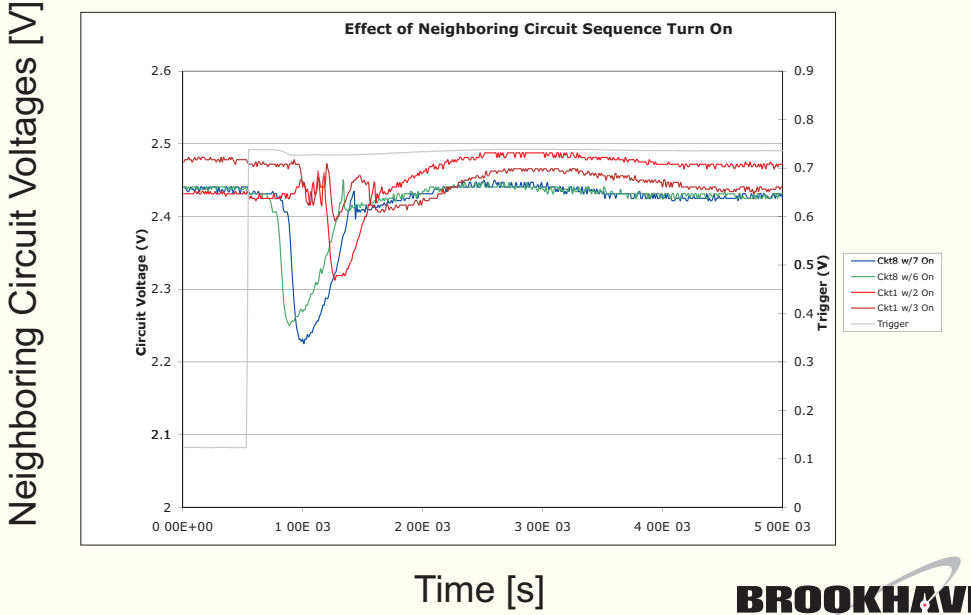
Sequential Power-Up



~ 800 mA (on 2.5 A nominal) current spike



~ 200-300 mV coupling to neighbors



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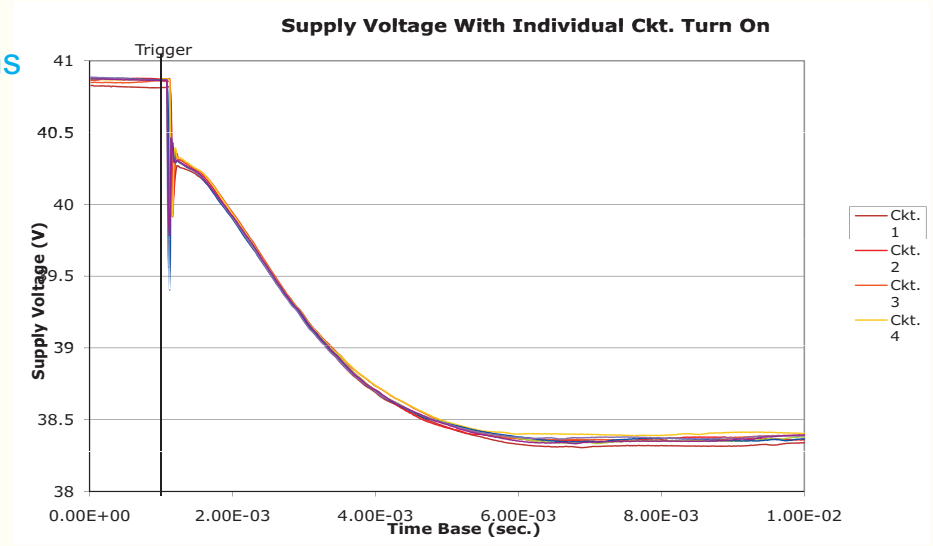
Slow Control Bypass System Tests

Test Condition: Toggle bypass for each hybrid, leaving all other hybrids on; I_s = 2.5A

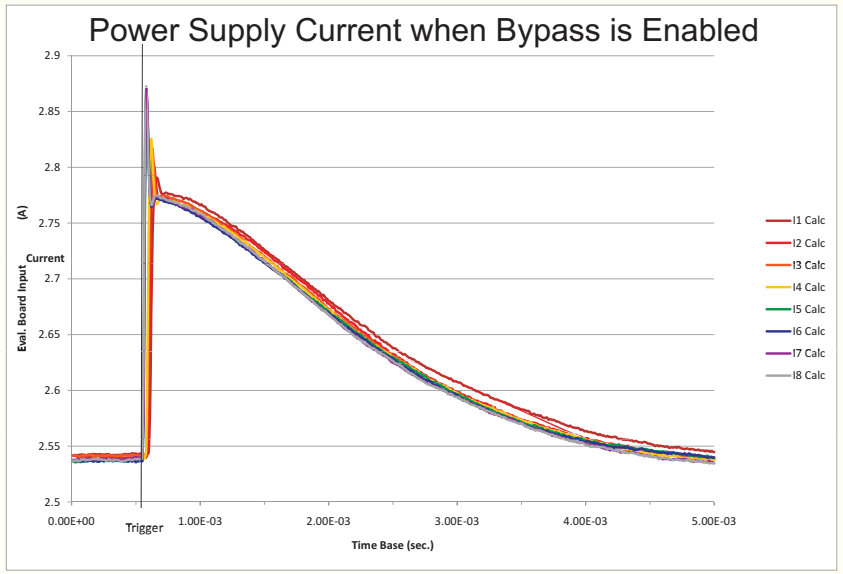
Observations

- Supply voltage adjust +/- 2.5 V as expected, settle time < 10 ms
- Little dependence of system response to which hybrid in chain is being toggled.
- Toggling bypass does not latch any real-time latches in system
- Maximum peak-to-peak spike in a neighboring hybrid's voltage is < 100 mV and settles in less than 5 ms

Conclusion: System is well behaved with regards to single hybrid bypassing with remaining hybrids in operation

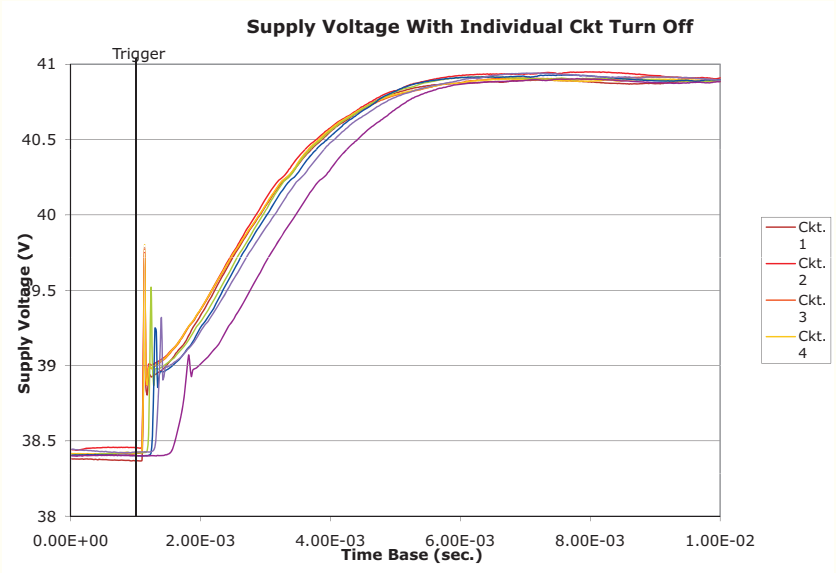


Time [s]



Supply Current [A]

Time [s]



Supply Voltage [V]

Time [s]

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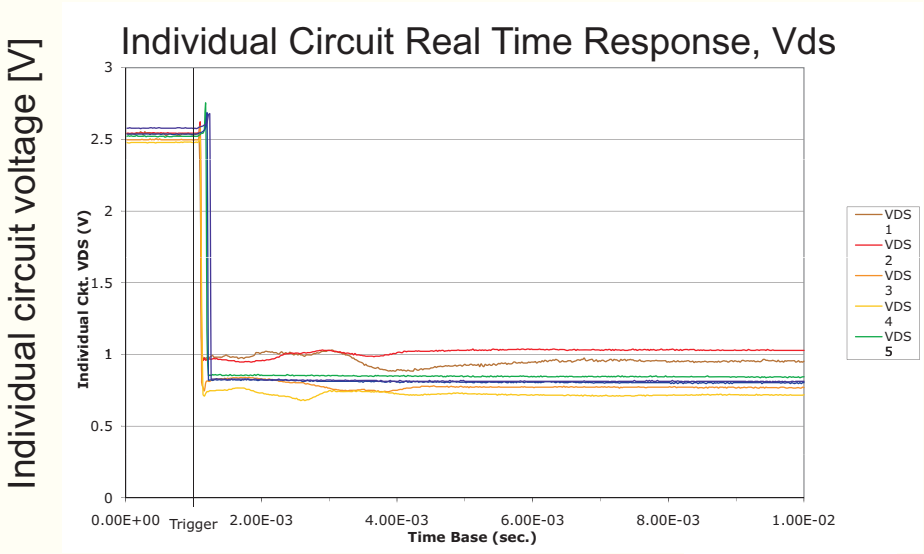
Real-Time Latch Tests

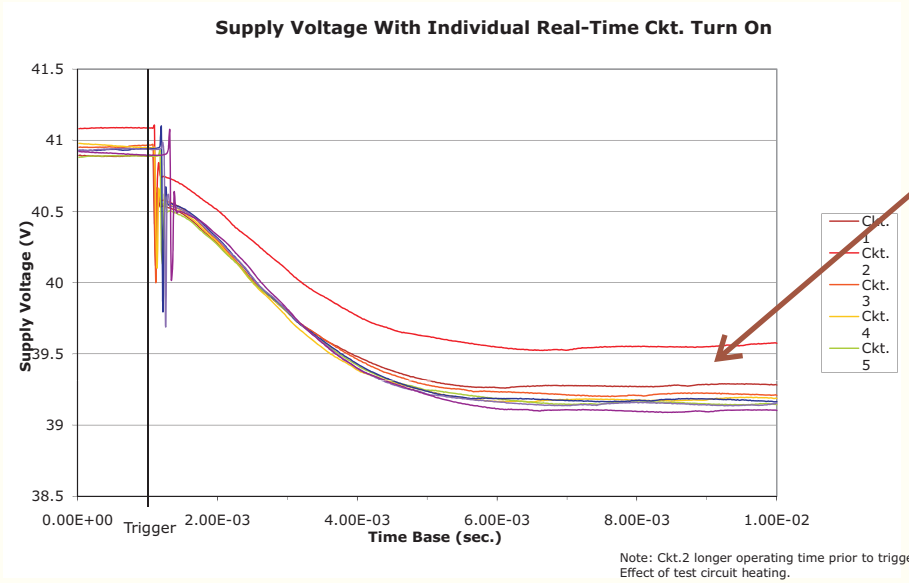
Test Condition: Open switch to single hybrid, leaving all others hybrids on; I_s = 2.5A
(mimics fused bond wires to hybrid)

Observations

- Supply voltage adjust - 1.7 V as expected (one exception), settling time < 10 ms
- Little dependence of system response to which hybrid in chain is being toggled.
- Triggering latch does not latch any other real-time latches in system
- Can re-enable hybrid by first enabling slow control bypass and then disabling

Conclusion: System is well behaved with regards to single hybrid latching with remaining hybrids in operation





Note: Ckt.2 longer operating time prior to trigger.
Effect of test circuit heating.

This board behaves differently; likely due to different FET threshold

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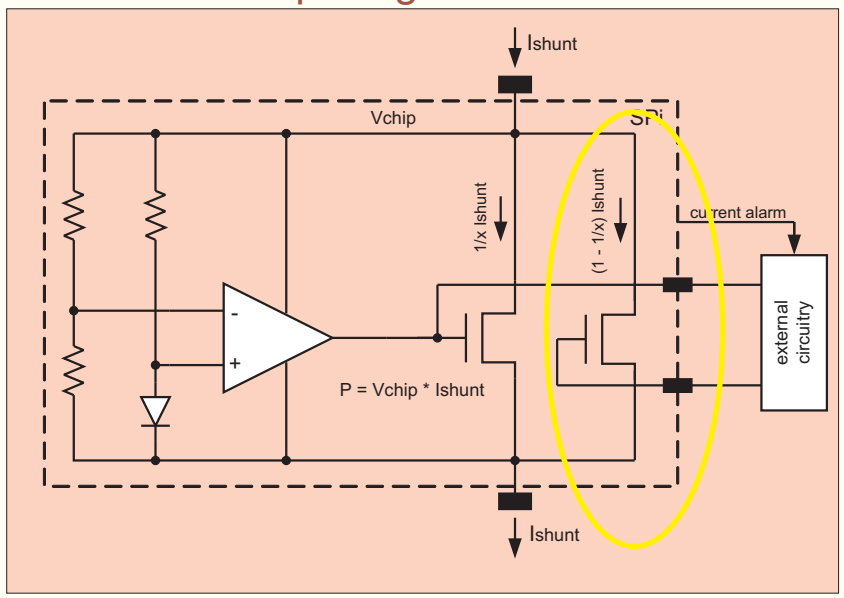
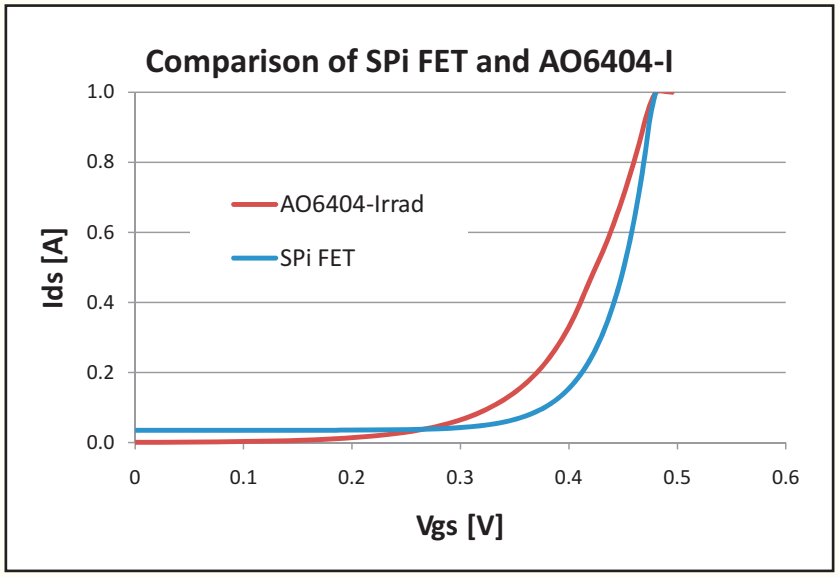
Elements for a Radiation Hard ASIC

Spi Regulator



High current FET in SPI chip was demonstrated to be radiation hard (60 Mrad) and could function as the slow control bypass FET in the power protection circuit (”The Spi chip as an integrated power management device for serial powering of future HEP experiments”, M. Trimpl et al, Proceedings of Science, Vertex 2009)

Drawing taken from M. Trimpl’s presentation “Serial Powering for Front End Electronics”, 7th International Meeting on Front-End Electronics, May 18-21, 2009, Montauk, NY, USA



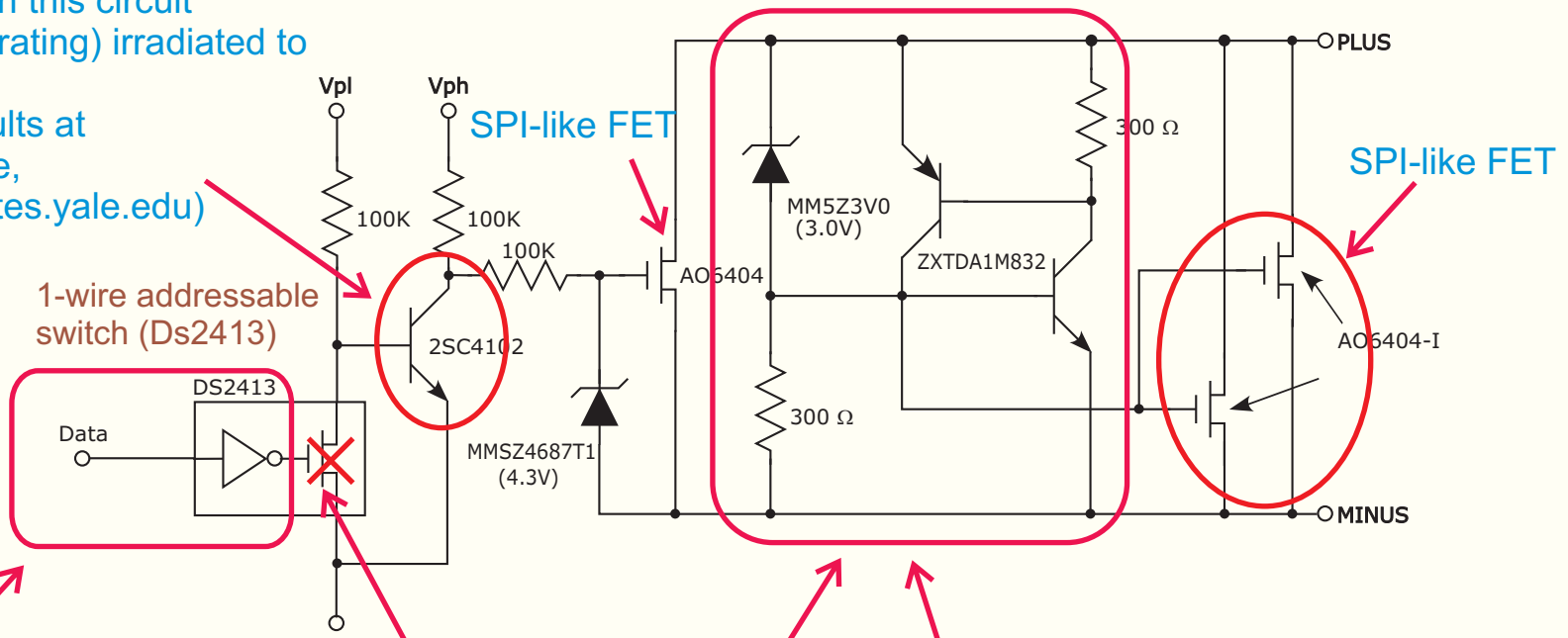
We use the irradiated Ao6404 in our prototype circuits as an approximation to a low threshold, high current, and radiation hard FET as typified by the Spi-FET.

Radiation Hard ASIC Implementation

High f_t NPN or GaN FET (GaN EPC1012 (200V rating) successfully tested in this circuit and EPC1015 (40V rating) irradiated to 60 Mrad at BNL.
See preliminary results at S. Dhawan's website, http://shaktipower.sites.yale.edu)

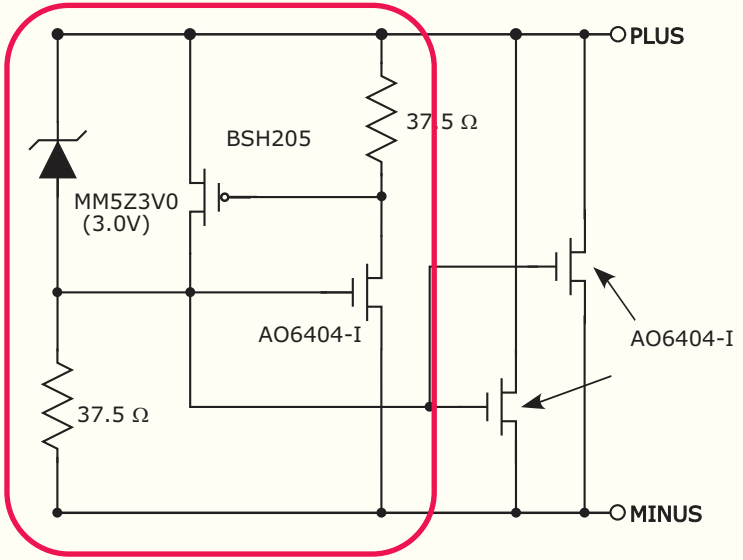
DCS Enabled Bypass (V_{ds} < 100 mV)

Real-Time Bypass (V_{ds} < 800 mV)



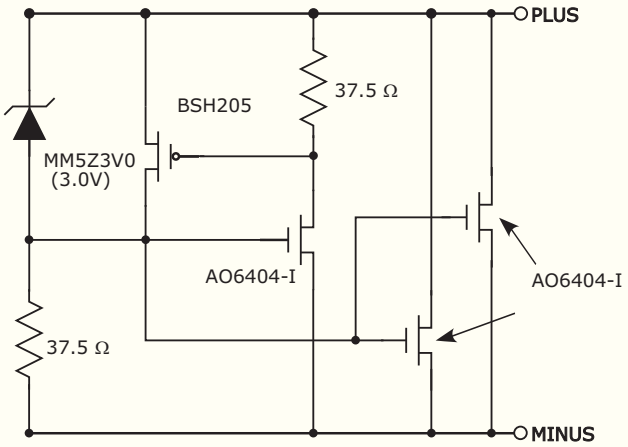
Straightforward low voltage ASIC Implementation

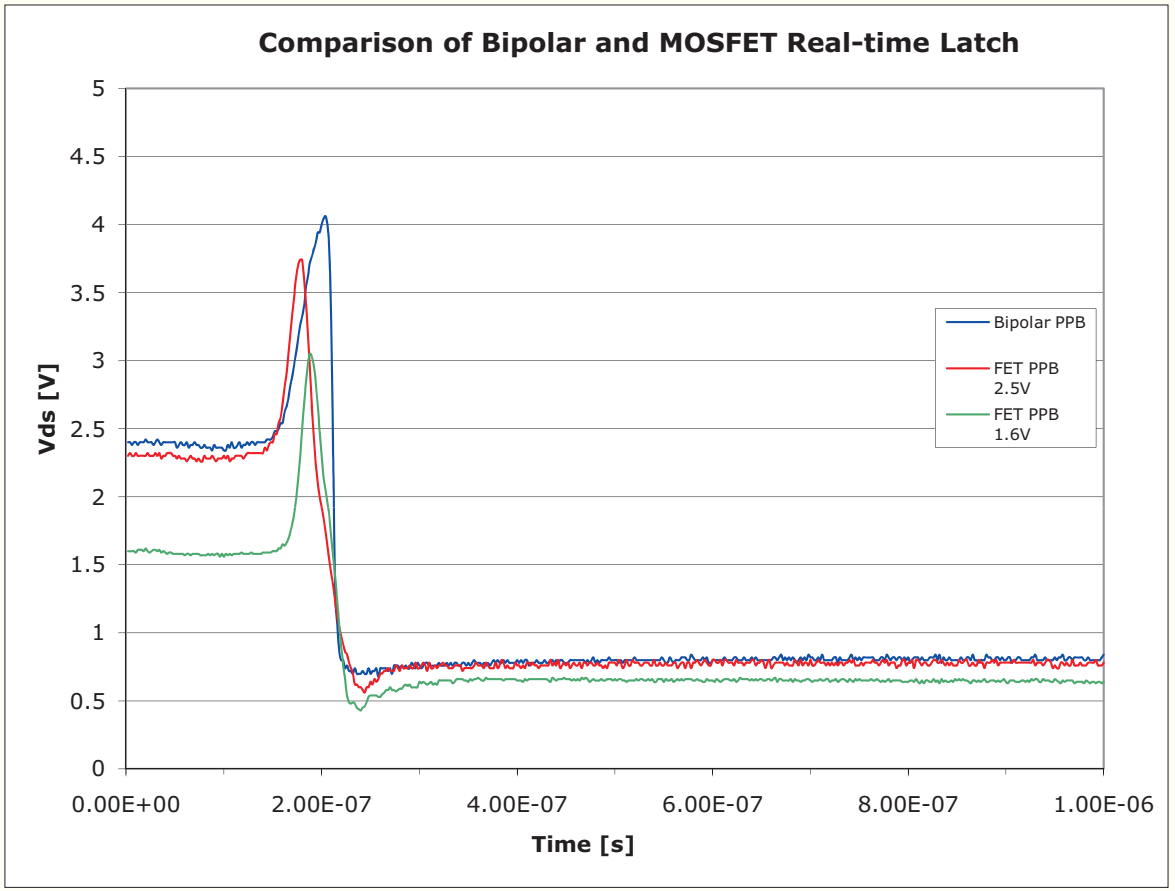
Not needed



Replace bipolar latch with low threshold radiation hard MOSFET latch. (Commercial MOSFET BSH205 is a relatively low threshold (~ 0.7V) FET useful for prototyping purposes)

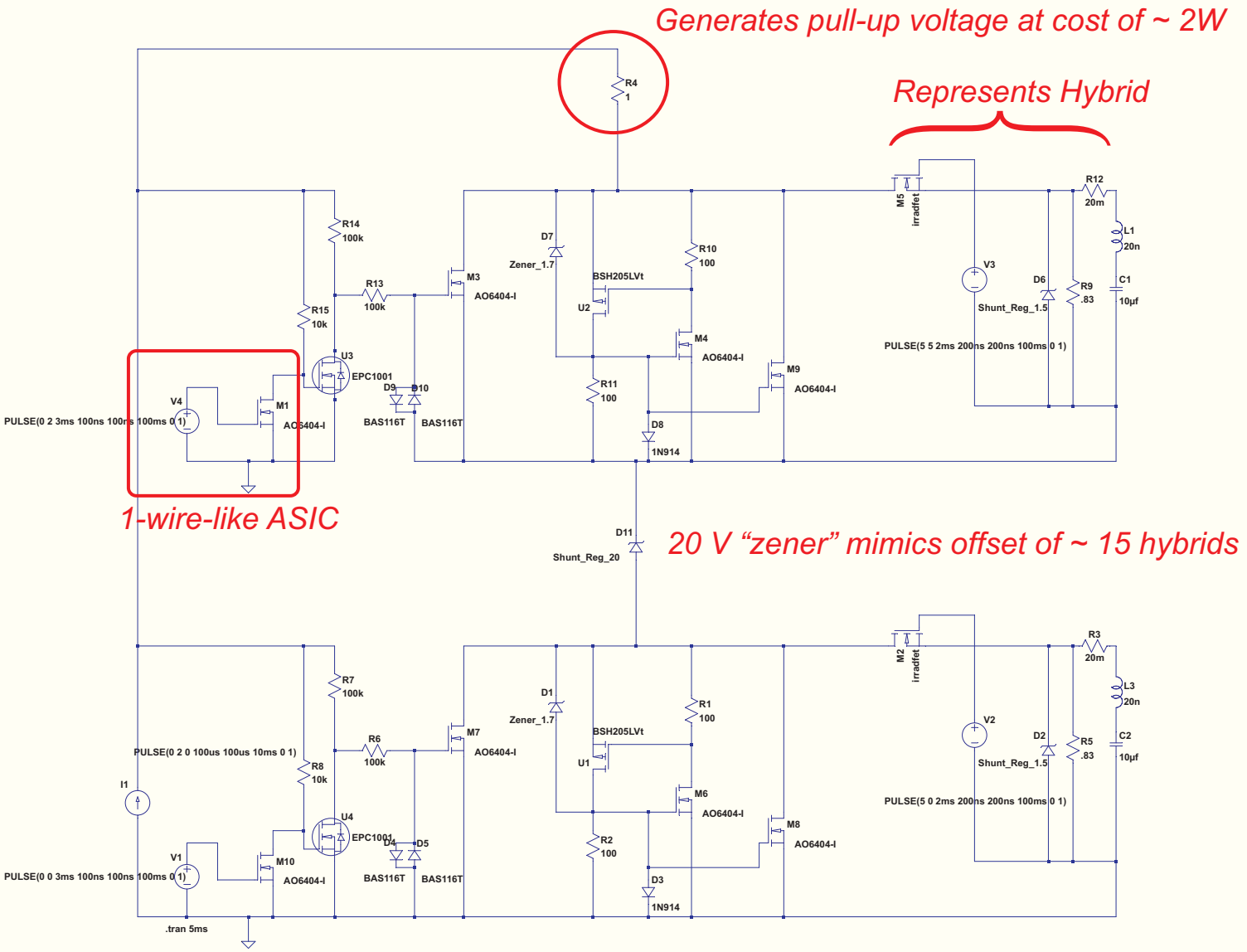
Bipolar and MOSFET Real-Time Latch Response





- MOSFET latch response similar to NPN-PNP response
- MOSFET latch tested at 2.5V and 1.6V (but used lower threshold LED to replace zener at 1.6V)

Elimination of Pull-Up Voltages



- Low threshold FETS (like Spi-Fet) and lower ABC-130 um chips permit elimination of pull-up voltages
- Circuit above results on hybrids being normally-on upon power-up (normally bypassed is equally possible but probably undesirable)

Summary

- An approach to protecting a serial power chain in the event of hybrid failures has been defined
- Based upon this definition a discrete power protection circuit (PPB) has been developed
- The circuit behaves uniformly as expected in single board testing
- System tests successful. No unexpected or undesired behavior is observed
- The PPB is being tested on the first Atlas Stavelet. Only slow control bypass is likely to be tested (the real-time latch will only be activated if there is a hybrid open failure)
- A radiation hard ASIC with a few supporting components is possible
- The circuit may be further streamlined (elimination of pull-up voltages)
- As Atlas requirements are better understood, we will pursue an ASIC implementation