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A 16:1 Serializer ASIC for Data Transmission at 5 Gbps

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A high speed, low power 16:1 serializer is developed using a commercial 0.25 μm silicon-on-sapphire CMOS technology. It operates from 4.0 to 5.8 Gbps in the lab test. Its total jitter is measured to be 62 ps and the bathtub scan demonstrates a 122 ps opening at BER of less than 10-12 level at 5 Gbps. The measured power consumption is 507 mW at this data rate. A proton test of this chip is scheduled in June and test results will be discussed when available.

Summary

The upgraded of ATLAS Liquid Argon (LAr) calorimeter readout upgrade calls for an optical link system of 100 Gbps per front-end board (FEB). A high speed, low power, radiation tolerant serializer is the critical component in this system. A commercial 0.25 μm silicon-on-sapphire CMOS technology has been evaluated to be suitable for development of radiation tolerant ASICs for particle physics front-end readout systems. Based on this technology we developed a 5Gbps 16:1 serializer as the first prototype chip for this system.

The serializer consists of a serializing unit, a PLL clock generator and a CML driver. The serializing unit receives 16 bit parallel LVDS data and output serial data in CMOS signal. It is composed of a cascade of 2:1 multiplexing circuit based on a static D-flip-flop for its better SEE immunity. In this design only the last 2:1 multiplexing stage is optimized to work at 5 Gbps or the highest speed. Two complimentary 2.5 GHz clock signals are required to speed up the D-flip-flop in this stage. The PLL clock generator based on a differential ring oscillator provides up to 2.5 GHz clock signals to serializing unit with 312.5 MHz reference clock. The PLL loop bandwidth is programmable to cope with different reference clock qualities. The CML driver is developed to drive the serial data signal from serializing unit to transmission line with 50 ohm impedance.

The prototype chip has been characterized in lab and the results indicate that it meets or exceeds its design goal. With a 27-1 PRBS data input at 312.5 MHz, the output signal, with a 1.1 V pk-pk amplitude and at 5 Gbps, is measured to have a rise and fall times of 52 ps. An eye mask test at 5 Gbps and a bathtub scan indicate an eye opening of 70% and 122 ps between BER less than 10-12. Random and deterministic jitters in the serial bit stream are measured to be 2.6 ps and 33.4 ps respectively. Power consumption is measured to be 507 mW at 5 Gbps. The serializer chip also passes the BER test at 10-12 level in the data rate range from 4.0 to 5.8 Gbps.

We single out the CML driver used in the serializer to probe the highest possible driving speed with this design. Tests on this driver indicates that it can work up to 8 Gbps without transmitting side pre-emphasis or a receiver signal equalizer . With our newly developed VBERT we are able to add a signal equalizer at the receiving end and the transmitted data rate goes up to 11 Gbps, indicating that this CML driver design is suitable for 10 Gbps data transmission. We plan to add pre-emphasis in the CML driver in the next 8-10 Gbps serializer design which will compose a 6-lane serializers chip to archive 40 to 50 Gbps data rate with one of six fibers as redundancy.

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