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Front end electronics for silicon strip detectors in 90nm CMOS technology; advantages and challenges

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We present a 16 channel front end prototype implemented in 90nm CMOS IBM process and optimized for 5pF input capacitance. A primary motivation for this project is to study the usefulness of the CMOS technologies below 130nm for front end amplifiers optimized for short strip silicon detectors on Super LHC experiments. On the example of presented design we will show critical aspects of the front end stages implemented in the deep submicron technologies. Particular effort has been put on the minimization of the power consumed by the front end electronics. The nominal power consumption providing ENC level below 800e- for the chip loaded with 5pF input capacitance is around 220uW per channel.

Summary

The delay of the schedule for the Super LHC experiments postpones the design and production of the front end ASICs for the upgraded detectors. Today it is not obvious if 130nm CMOS technology used now in many research upgrade programs will be still leading edge technology for HEP at the moment of Super LHC. It is therefore reasonable to start evaluation of CMOS technologies below 130nm from the point of view of its usefulness for front end electronics for the future detectors. One of the challenging applications is the development of the front end electronics for silicon trackers where the important issue is very high occupancy impacting final granularity of the system and number of electronic channels. The primary concern is the minimization of power consumption keeping the rest of the analogue parameters like speed, noise and dynamic range as well as radiation resistance at the required levels. Although technology scaling offers many advantages related to increased transconductance and higher ft of the devices, the short channel effects and lower intrinsic gain of the transistor present challenges for the input stages designed for detector capacitances of the order of few pico Farads. In the paper, on the example of the prototype front end implemented in IBM CMOS 90nm process, we identify critical points of such design and give some solution to obtain desired performance of the circuit.

The sixteen channel front end prototype consisting of preamplifiers, shapers and discriminators readout through digital output multiplexer allows for detail study of the gain, noise and speed parameters as well as for the examination of discriminator matching. In addition we implement a test channel permitting for direct analogue measurements of signals at the output of preamplifier, shaper and discriminator stages. The preamplifier stage has been optimized for 5pF input capacitance and it is built with NMOS input transistor employed in regulated cascode structure and loaded with regulated cascode current source. Using this method, with the intrinsic gain of the single transistor around 18V/V, we are able to obtain roughly 70dB open loop gain together with 3.5GHz Gain Bandwidth Product what provide good characteristic of the input impedance and satisfactory Power Supply Rejection Ratio. The intrinsic peaking time of the shaper is 22ns what keeps the time walk of the comparator better than 12ns for 0.25fC signal overdrive. The analogue gain at the discriminator input is around 100mV/fC and the good linearity is kept up to 6fC. Keeping in mind that the power supply in 90nm technology is 1.2V and practically all of the amplifying stages work in cascode configuration the obtained dynamic range is very satisfactory. For the nominal 100uA bias of the input transistor and the front end loaded with 5pF detector capacitance the simulated ENC level is below 800e- what allows for operation with heavily irradiated silicon detectors. The overall nominal current consumed by the full chain is around 180uA what for 1.2V power supply converts to 220uW power consumption in a single channel. The prototype has been submitted to the foundry in February 2010 and it is expected back soon.

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