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A 4.9-GHz Low Power, Low Jitter, LC Phase Locked Loop

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An LC phase locked loop ASIC, fabricated in a commercial 0.25-μm Silicon-on-Sapphire CMOS technology, has been characterized in lab. Random jitter and deterministic jitter are less than 2.5 ps and 10 ps, respectively. The power consumption at 4.9 GHz is 218 mW. The measured tuning range, from 4.7 to 5.0 GHz, is narrower than the simulated values of from 3.8 to 5.0 GHz. The narrow tuning range has been investigated and traced to the first stage of the divider. This will be corrected in the next submission. A test with a proton beam is scheduled in June.

Summary

A low power, low jitter, LC phase locked loop (PLL) has been designed for a serializer with six-lanes and 8-10 Gbps each lane, targeting for the upgrade of the ATLAS Liquid Argon Calorimeter readout system which calls for a data transmission of about 100 Gbps per front–end board (FEB) with power consumption of less than 20 W. The PLL has been characterized in lab and a proton beam test is scheduled in June. The lab test results are presented here. Irradiation test results will be reported when available

The PLL is fabricated in a commercial 0.25-μm Silicon-on-Sapphire (SoS) CMOS technology. The PLL consists of a voltage control oscillator (VCO), dividers, a phase frequency detector (PFD), a charge pump, and a second-order low pass filter. The VCO uses on-chip spiral inductors and NMOSFET varactors as the LC tank. The dividers consist of four stages of divide-by-2 circuit. The first stage is a common-current-logic (CML) and the following stages are CMOS.

Four ASIC dies have been tested. The Random jitter and deterministic jitter are less than 2.5 ps and 10 ps, respectively. The power consumption at 4.9 GHz is 218 mW. The output amplitude is no less than 0.98 V.

The measured tuning range, from 4.7 to 5.0 GHz, is narrower than the simulated values, from 3.7 to 5.0 GHz. The mismatch has been investigated and the problem has been traced to the first stage in the divider chain. The problem is verified in the simulation and confirmed by testing a separate divider implemented in the same ASIC. This failure mechanism is understood. When the control voltage to the VCO decreases, the common mode voltage of VCO output increases. Consequently, the leakage current of CML latches in the divider increases and causes the CML latches become unstable, resulting in spikes in the divider output. This problem will be corrected in the next submission.

Since no varactor model has been provided in the design kit, we implemented a NMOSFET varactor in the same ASIC. The measured capacitance is higher than the simulated value, though the trend of measured C-V curve is consistent with that of simulated curve. This excludes that the inaccuracy of the varactor model is the cause of mismatch of tuning range. In the flat regions of each curve the simulated curve is absolutely flat, indicating that some minor effects have not been modeled in the simulation.

An irradiation test using 198-MeV proton beam is scheduled in early June and the test results will be presented in the workshop.

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