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Electronics and Cooling for the Silicon Vertex Detector of the Belle II Experiment

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A major upgrade of the KEK-B factory (Tsukuba, Japan), aiming a peak luminosity of 8 x 10^35 / (cm^2s), which is 40 times the present value, is foreseen until 2013. Consequently an upgrade of the Belle detector and in particular its Silicon Vertex Detector (SVD) is required. We will introduce the concept and prototypes of the full readout chain of the Belle II SVD. Its APV25 based front-end utilizes the Origami chip-on-sensor concept, while the back-end VME system provides online data processing as well as hit time finding using FPGAs. Furthermore, the design of the foreseen DSSDs, the mechanics and the cooling system will be discussed.

Summary

The new Belle II SVD will consist of four layers of double-sided silicon strip sensors at radii of 3.8, 8, 11.5 and 14 cm, completed by a double-layer pixel detector as the innermost sensing device. All DSSDs will be read out by the APV25 chip, which was originally developed for the CMS experiment. It has a peaking time of nominally 50ns, an integrated analog pipeline of 192 cells and has been proven to meet the requirements for Belle II in matters of occupancy and dead time. Since the KEK B-factory operates at relatively low energy, material budget inside the active volume has to be kept low to minimize multiple scattering.

We will present the concept of the readout electronics of the future Belle II SVD. Its front-end uses the APV25 readout chip arranged according to the Origami chip-on-sensor concept to ensure both low material budget and lowest possible amplifier noise. The VME back-end system not only digitizes the analog signals, but also provides on-board data processing and sparsification. It further allows to determine exact hit timing with a precision of a few nanoseconds by taking six consecutive samples of the APV shaper output signal. Thanks to this feature, hits from background particles can be identified and discarded, which finally leads to a significant occupancy reduction. Even though the development of the readout electronics is still ongoing, we have successfully tested its building blocks on prototypes in several beam tests and the lab.

In 2009, the principle feasibility of the Origami concept has been shown by building a prototype module using a 4" DSSD. Recently, new Belle II sensors (6") were delivered, and we are now assembling an Origami module for this full size sensor. Later this year, we want to build a full ladder of the outermost layer, as this will be the most complicated object and by demonstrating its producibility we thus prove the concept of the whole Belle II SVD. Starting from the assembly steps of the 2009 prototype, we will further elaborate and refine the procedure, aiming at a mechanical precision in the order of few 10um.

The Origami concept requires a sufficiently powerful, but low mass cooling system inside the active volume of the detector. As all APV chips of a ladder are aligned in a row in the Origami concept, cooling can be done by a single thin pipe. Measurements have shown that the signal-to-noise ratio can be improved by about 20% compared to room temperature by using a coolant at sub-zero temperatures. Hence, we plan to operate the APV chips at about -20℃ using either a liquid or two-phase CO2 system. Considerations on the cooling system have been started recently, accompanied with the design of the mechanical ladder structure. Although the design presently is in a very early stage, we plan to present a first concept of the cooling system at the TWEPP workshop in September 2010.

Key words:
APV25, Silicon Detector, DSSD, Chip-on-Sensor, Origami, Belle II, SVD

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