



The ALICE Silicon Pixel Detector: Commissioning and Optimization of the Detector Performance

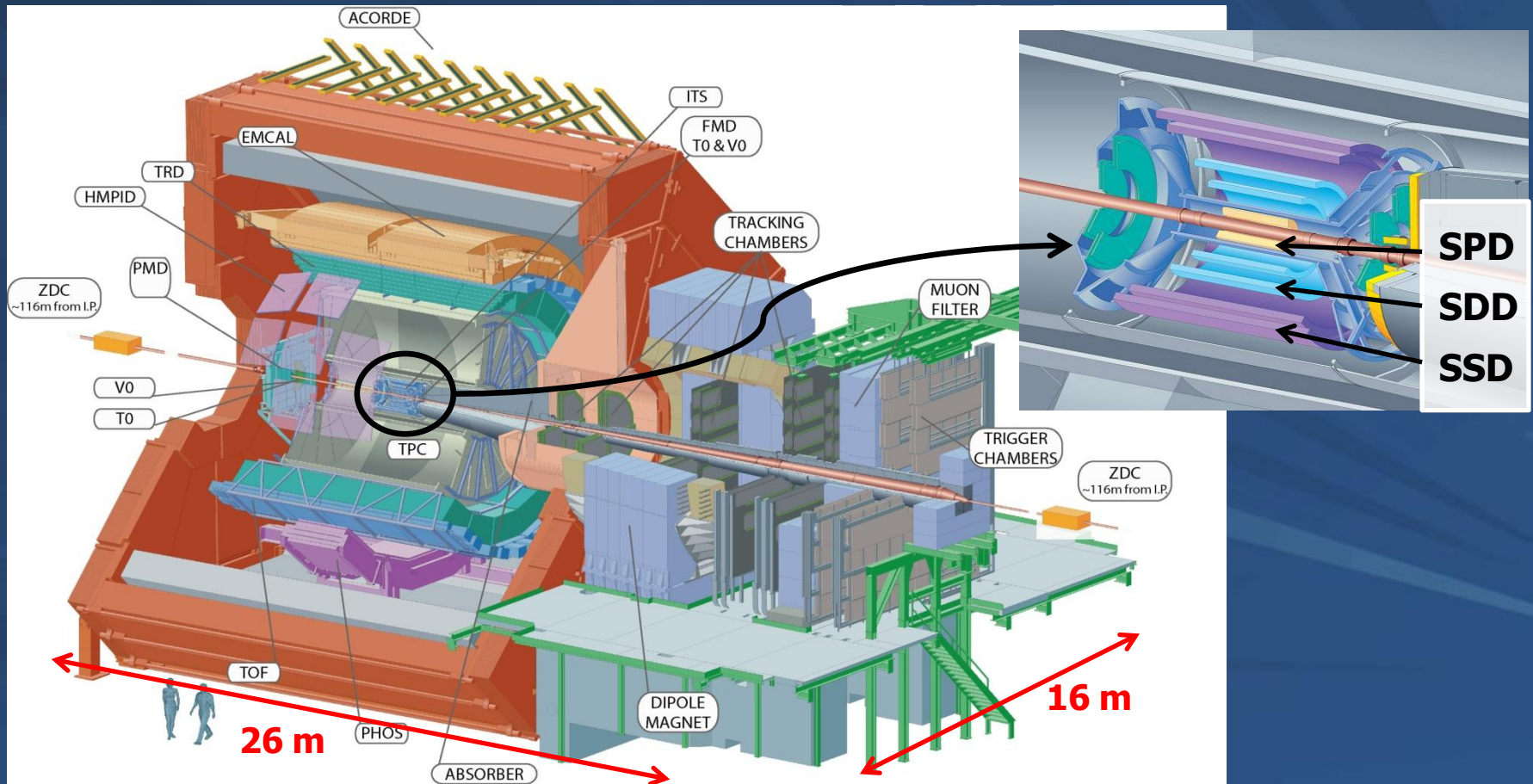
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CERN – European Organization for Nuclear Research
on behalf of the SPD project in the ALICE Experiment

ALICE Inner Tracking System

- experiment designed for heavy ion collisions (Pb-Pb @ 2.75+2.75 TeV per nucleon)
- 3 different silicon detector technologies in 6 barrel layers
- **Pixels** (SPD), **Drift** (SDD), double sided **Strips** (SSD)



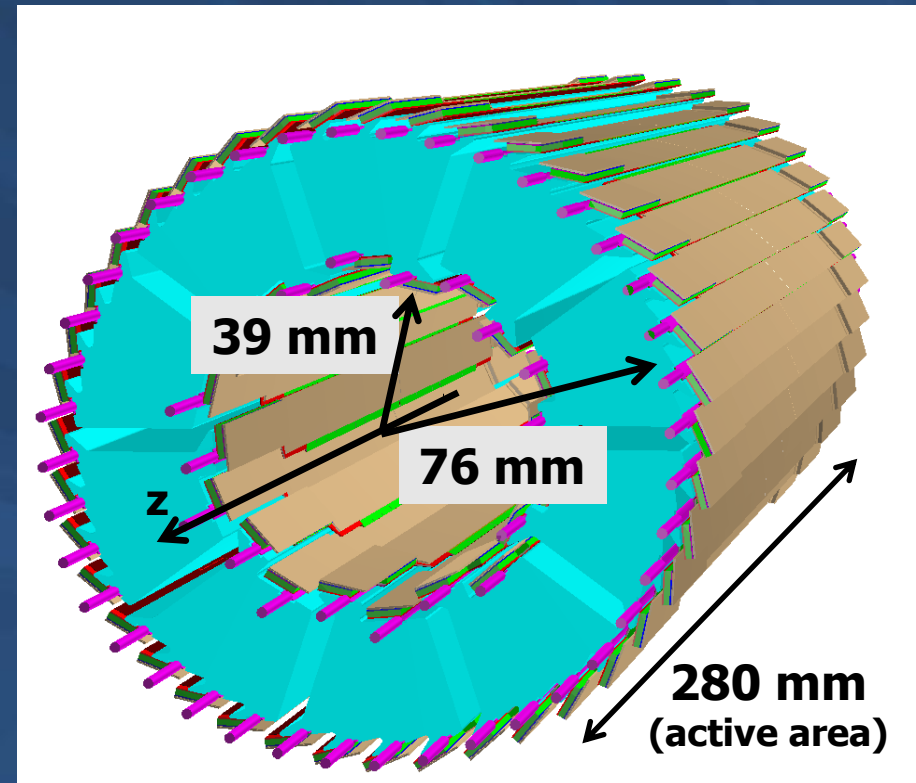
ALICE Silicon Pixel Detector

REQUIREMENTS

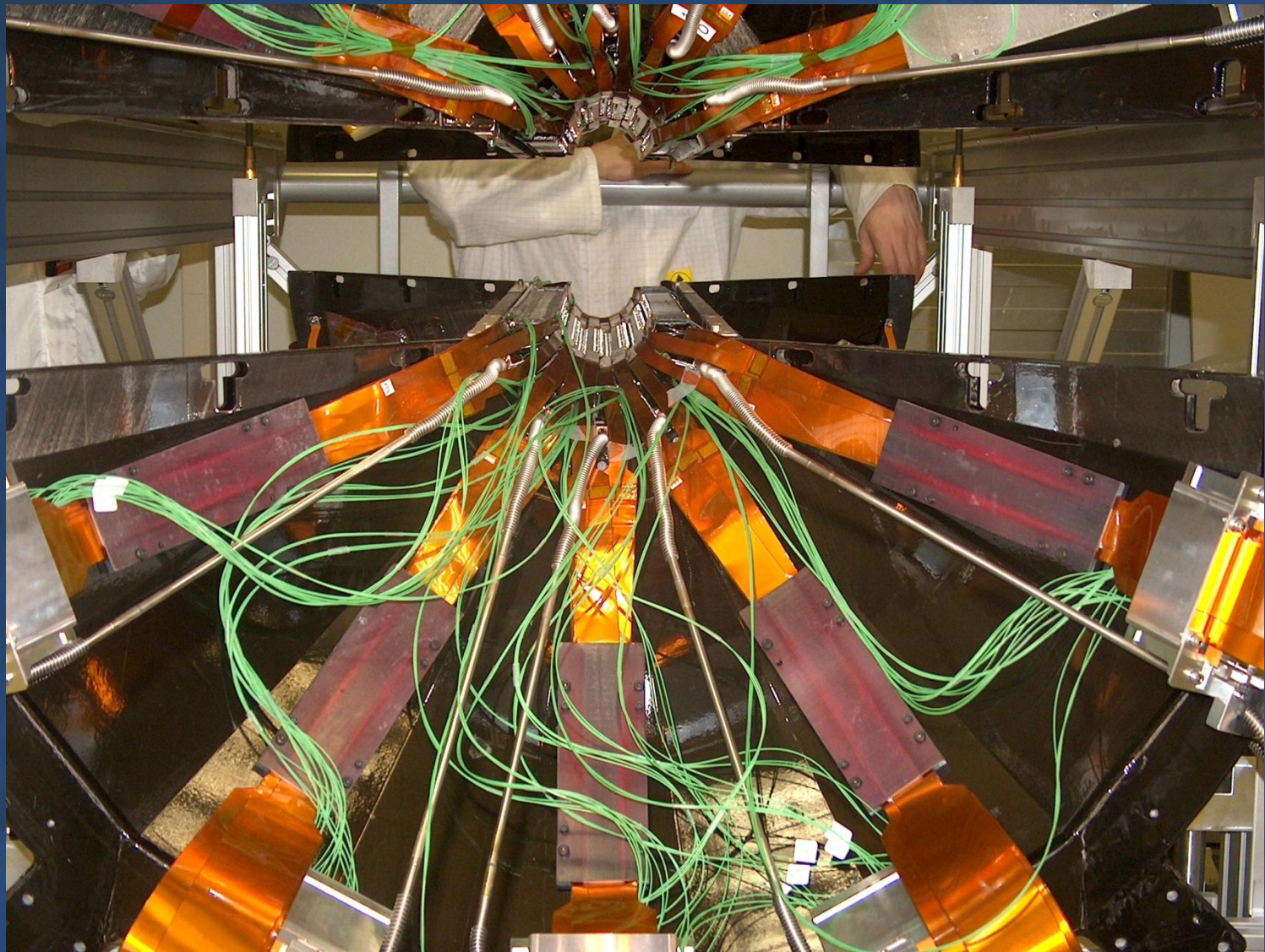
- fast matrix readout (256 μs)
- high detection efficiency ($> 99\%$)
- high spatial precision ($\sim 12 \mu\text{m}$ in the bending plane)
- stringent material budget ($\sim 1.1\% X_0$ per layer)
- prompt signal for L0 trigger

CHARACTERISTICS

- 2 innermost layers, 0.24 m^2
- $\sim 9.8 \text{ M}$ readout channels
- pixel size $425 \times 50 \mu\text{m}^2$ ($z \times r\phi$)
- readout chip $0.25 \mu\text{m}$ CMOS technology
- power consumption $\sim 1.35 \text{ kW}$



ALICE Silicon Pixel Detector



ALICE Silicon Pixel Detector



SPD	→	10 sectors
Sector	→	12 half-staves
Half-stave	→	1 multilayer bus → 1 MCM → 2 ladders
Ladder	→	1 sensor → 5 readout chips
Readout chip	→	8192 pixels

Total SPD components

10 sectors

120 half-staves

120 multilayer buses

120 MCM

240 ladders

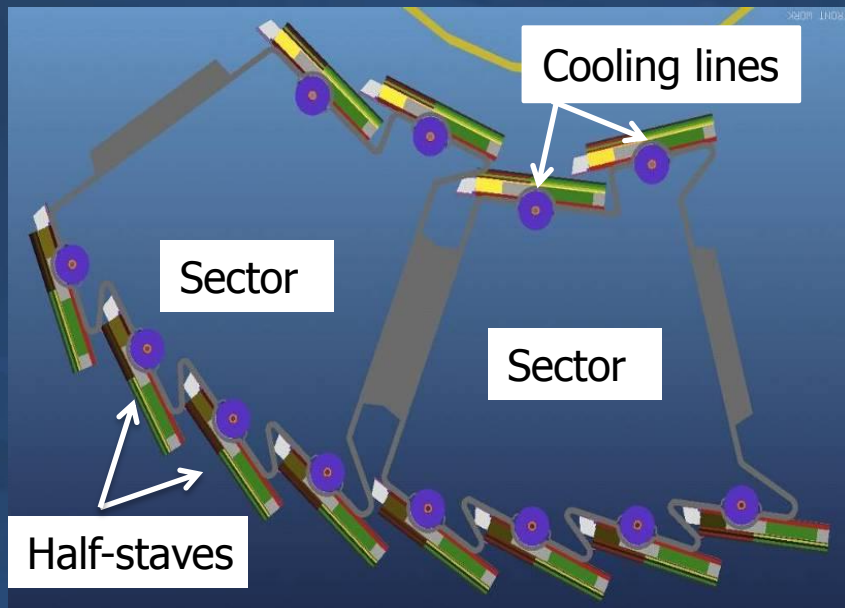
240 sensors

1200 readout chips

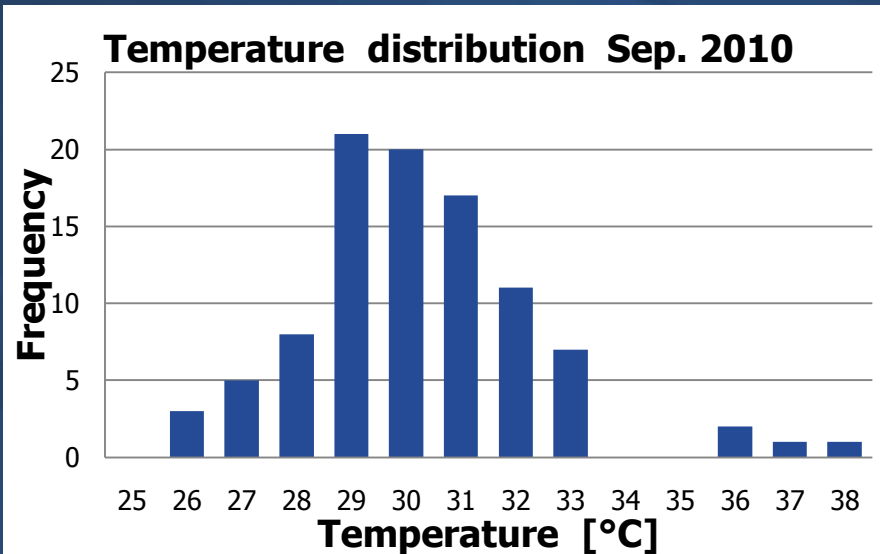
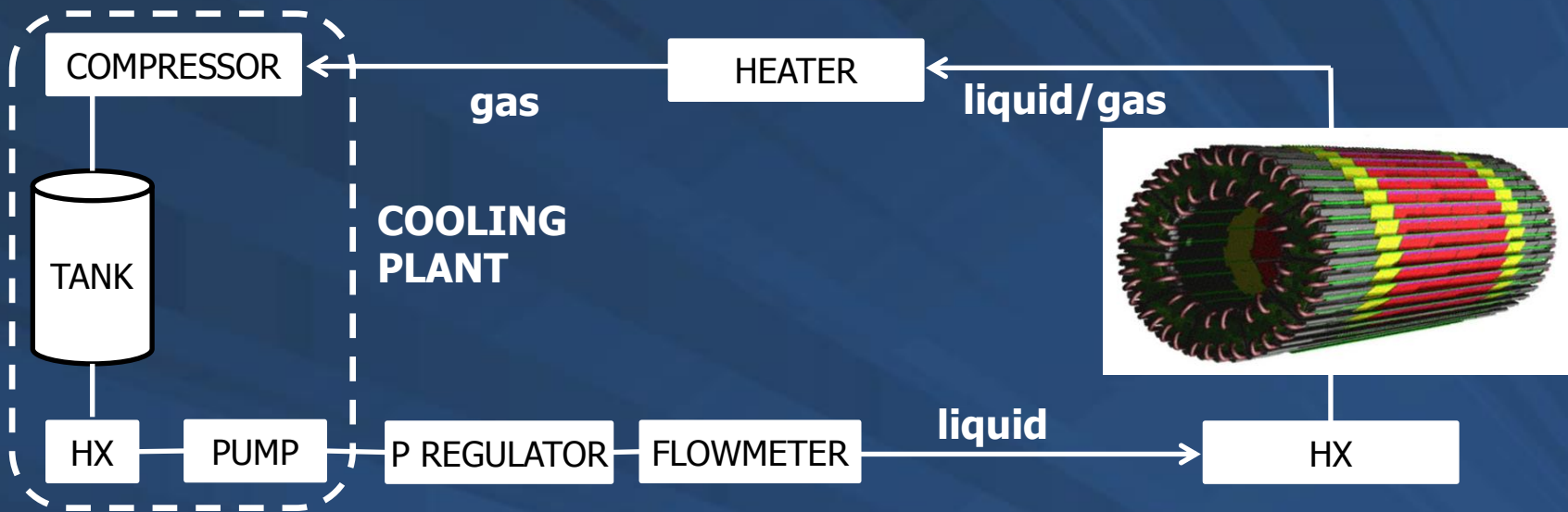
$\sim 9.8 \times 10^6$ pixels

SPD cooling system

- without cooling the SPD temperature would increase $\sim 1^\circ\text{C/s}$
- evaporative system with C_4F_{10} (dielectric, chemically stable, non toxic)
- capillaries under each half-stave, embedded in the carbon fiber support
- monitoring of T-p at the plant and up/downstream the detector
- control of liquid pressure per line (equivalent to flow)



SPD cooling system

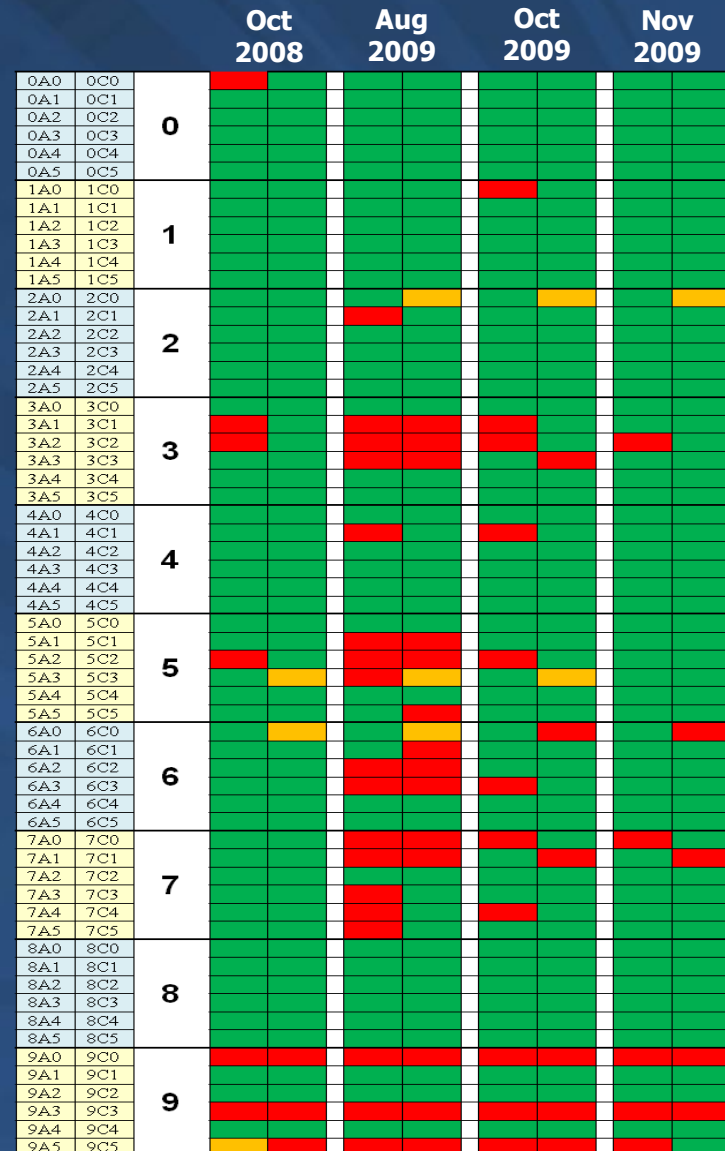


Improvements observed after the tuning of the cooling system

Avg. operating temperature:
29.8 °C

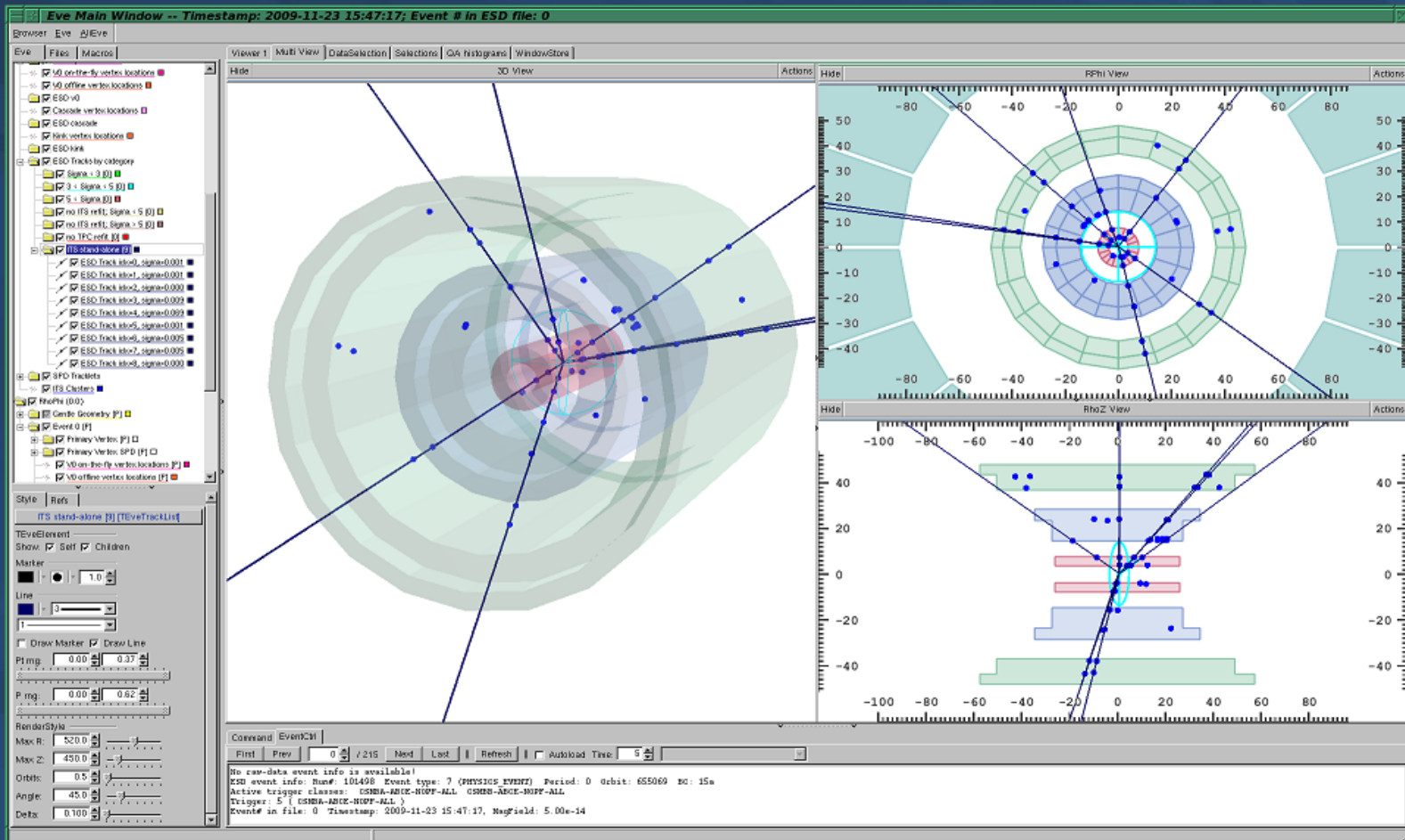
SPD cooling system

- commissioning started in 2007
- **Aug 2009:** after long shut-down
 - 85 HS ON (~71%)
 - actions taken:
 - counter-flow-wise cleaning
 - new input lines
 - more T/p monitors on all lines
 - flow gauges
 - per-line liquid pressure control
- **Oct 2009:**
 - 101 HS ON (~88%)
 - actions taken:
 - installation of subcooling
- **Nov 2009:**
 - 110 HS ON (~91.7%)
 - to keep the stability ~100 HS from then on



SPD cooling system

... BUT ... SPD is performing really well
First event @ 900 GeV



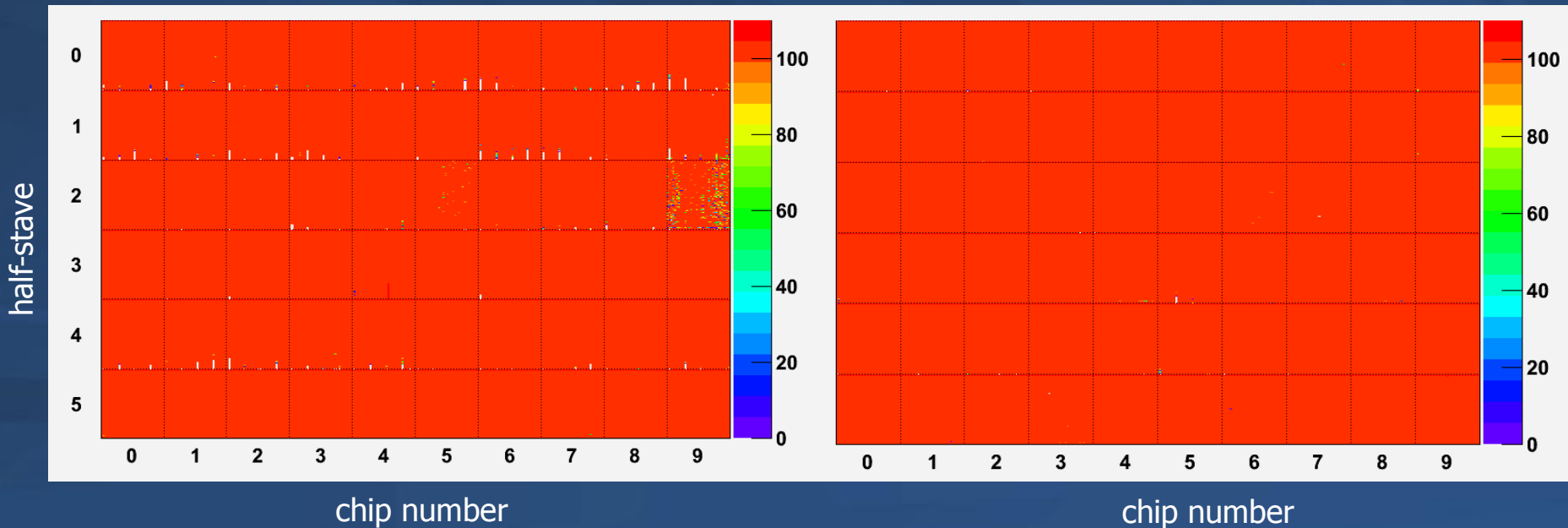
Uniformity of chip matrix

- checked noisy/inefficient regions with internal pulser of known amplitude
- injection tests and cosmic data accumulated for cross checking
- noisy pixels: $< 0.01\%$ (masked)

maps obtained with internal pulser
half sector 1 side C

BEFORE

AFTER

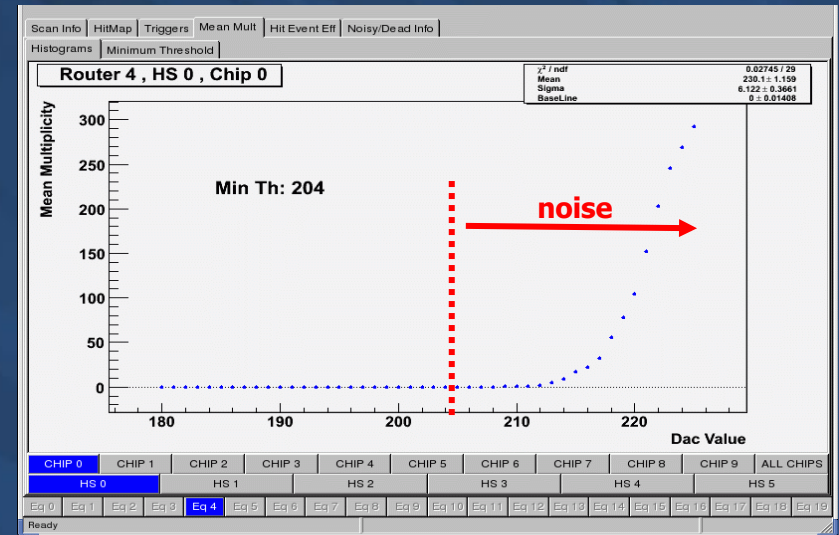


Threshold optimization

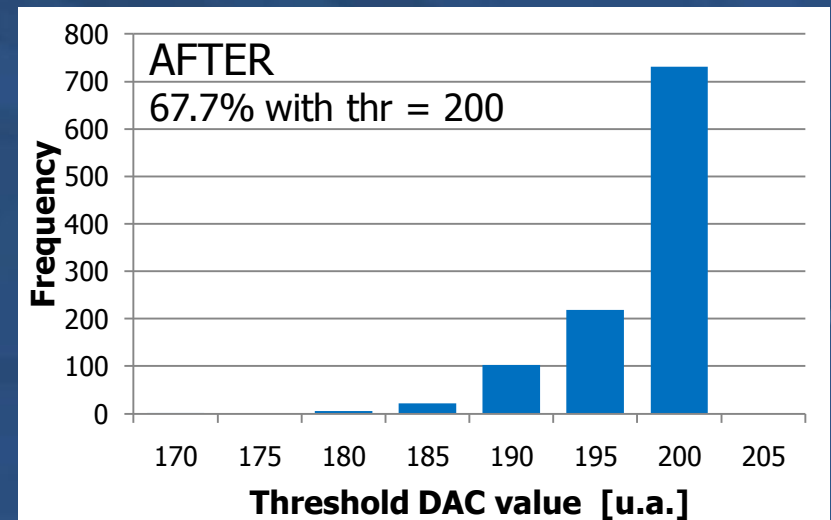
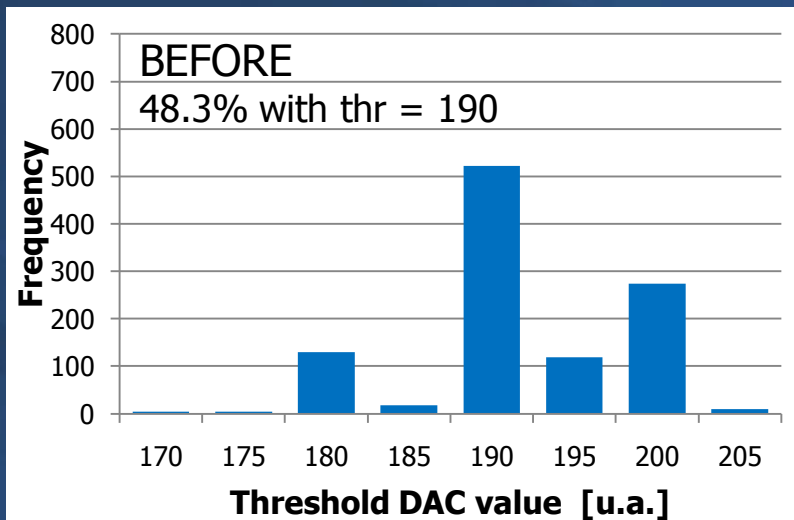
Minimum threshold scan

finds the lowest threshold value at which the chip can be operated without noise

- scans through threshold values
- finds the closest to the noise area
- applies a safety margin (5 steps)



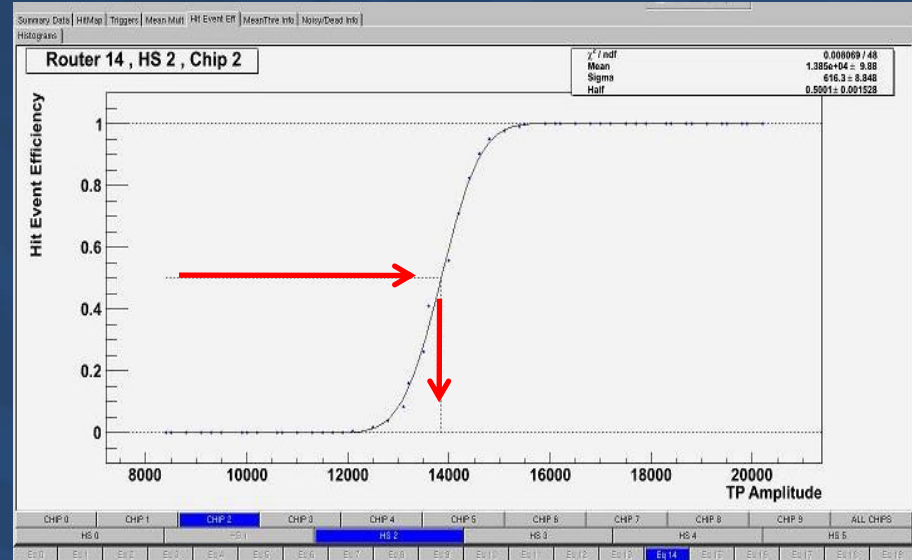
Distribution of threshold settings in the SPD



Threshold optimization

Mean threshold scan

- scans through different amplitudes of internal pulser
- determines an S-curve per pixel
- calculates the mean value and sigma per chip

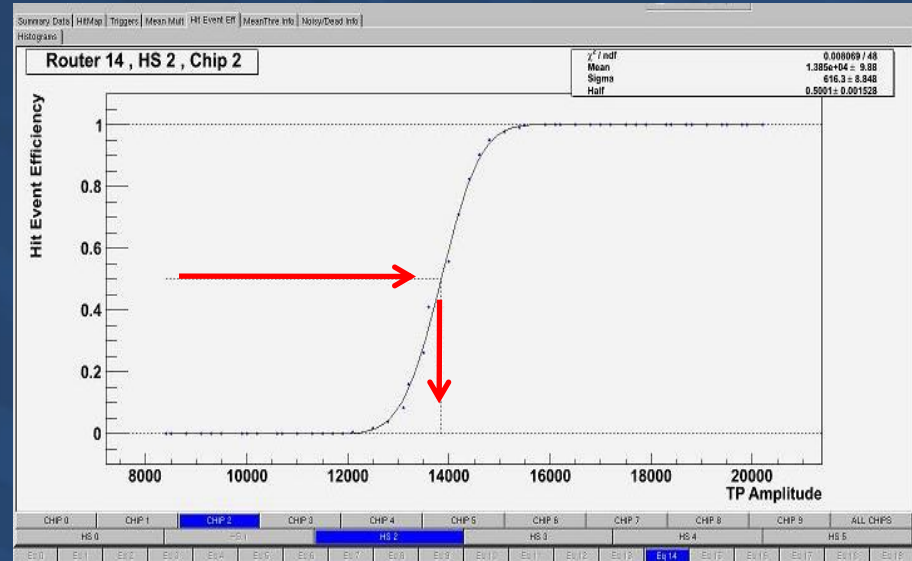


200	195	190	185	180	preVth
551	233	122	28	11	# of chips
30.0	33.0	35.2	37.4	41.3	mean
1.7	1.9	1.9	2.1	1.9	sigma

Threshold optimization

Mean threshold scan

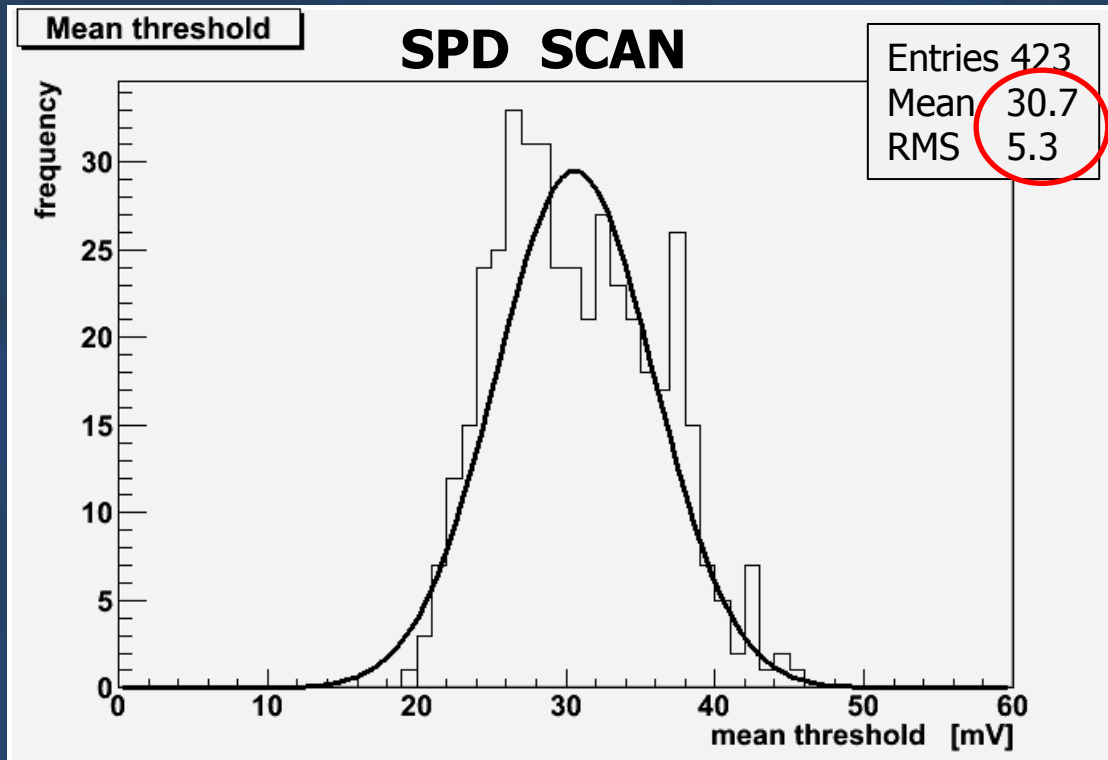
- scans through different amplitudes of internal pulser
- determines an S-curve per pixel
- calculates the mean value and sigma per chip



200	195	190	185	180	preVth
551	233	122	28	11	# of chips
1980	2190	2320	2470	2730	mean in electrons
110	120	120	140	120	sigma in electrons

Preliminary conversion:
conversion factor of $66 e^-/mV$
found from tests in the lab

Threshold optimization



SPD scan:

- selected only chips with
- threshold = 200 DAC
- preamp = 160 DAC

LAB tests:

- 5 half-staves
- same conditions

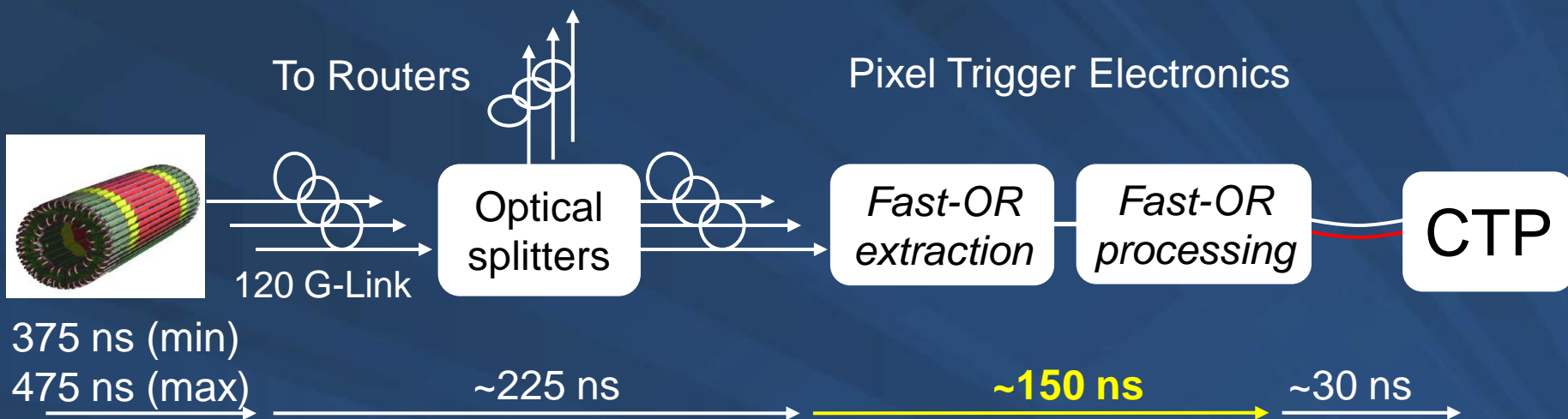
LABORATORY:

- mean: 29.7 mV
- RMS: 3.6 mV



Good agreement
between the two results

Fast-OR trigger signal

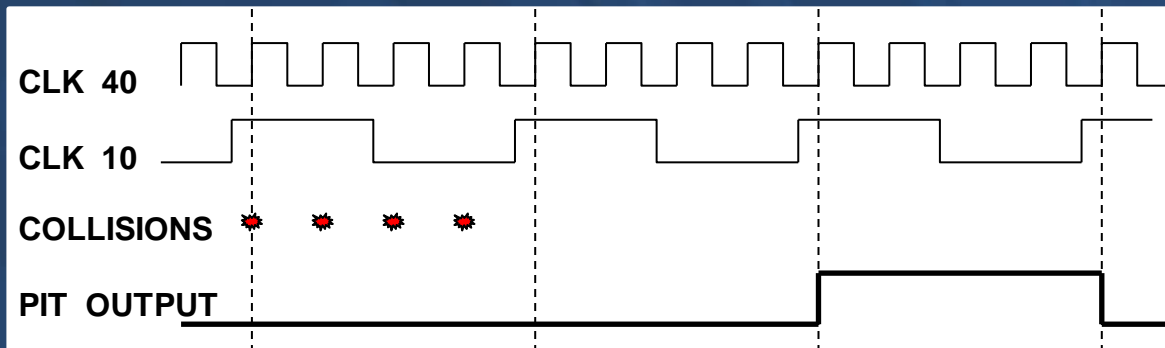


- contributes to the L0 trigger in ALICE
- Fast-OR active on registration of at least 1 hit per chip
- 10 chips/half-stave -> **1200 FO bits** every 100 ns on the optical G-Link
- overall latency = **780 ns (min) – 880 ns (max)**
- deserialization of data and Fast-OR bits extraction
- processing of the Fast-OR bits
 - up to **10 algorithms** executed at the same time (processing time = **25 ns!**)
 - minimum bias + multiplicity trigger for p-p collisions
 - centrality trigger for Pb-Pb collisions

Fast-OR efficiency

SPD clock (10 MHz) integrates 4 consecutive BCs

Evaluation of trigger efficiency for the single BCs before/after the SPD clock shift



IF (hit on 1 chip)
ANDIF (FO on same chip)



this chip is **efficient**

Data from 900 GeV and 7 TeV collisions

	Pos. 1	Pos. 2	Pos. 3	Pos. 4
before	99 %	99 %	99 %	80 %
after	99 %	99 %	99 %	97 %

Last BC position (Pos. 4) is the closest to SPD clock edge -> small jitters can cause inefficiency

Efficiency improved after the SPD clock shift

Fast-OR circuit calibration

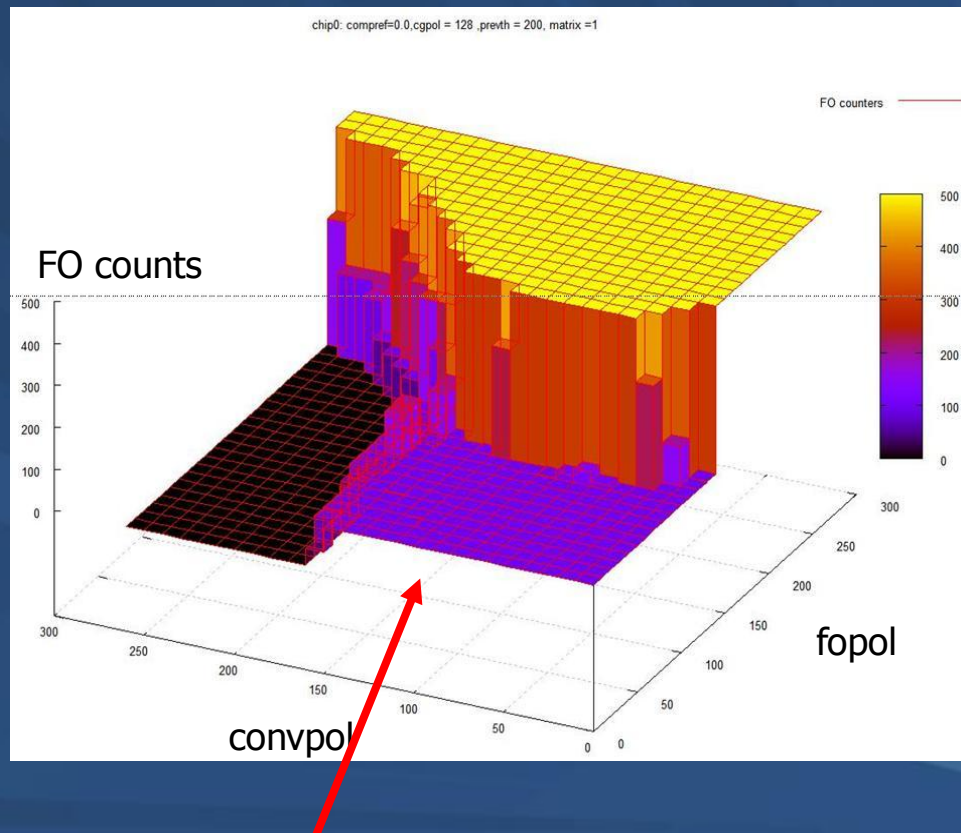
Dedicated circuitry in each pixel cell
Required tuning of 5 DACs for every of
the 1200 readout chips to

- maximize efficiency
- minimize noise

Automatic calibration procedure

- verifies Fast-OR efficiency in different operating conditions
- scans of the DAC values
- checks of the signal rates
- coordinates SPD readout, control system and PIT operation
- efficiency condition on Fast-OR signal: 100%

Example: 1 chip, central pixel
COMPREF = 0, Pre-VTH = 200



OK -- FO counts = # triggers sent = 100

Cosmic data

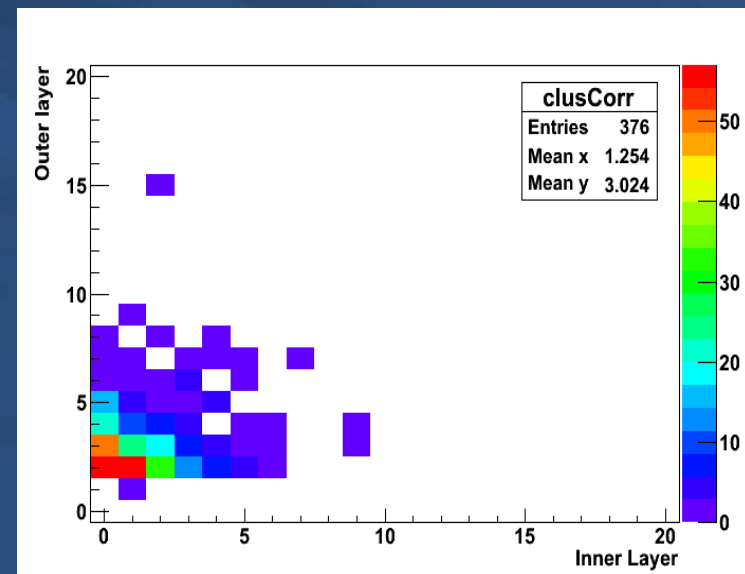
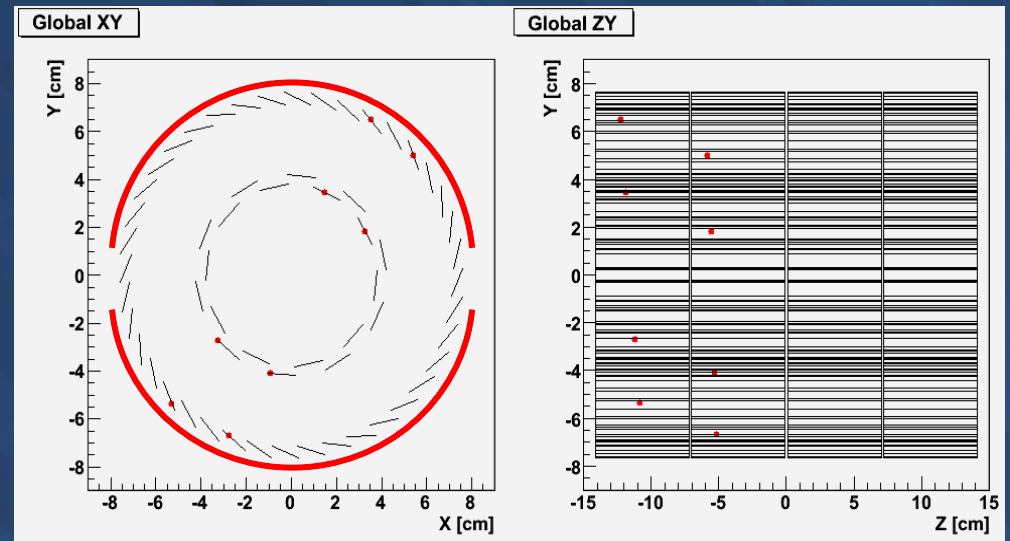
Pixel Trigger used as L0 trigger during ALICE commissioning with cosmic data

Coincidence algorithm: top/bottom outer layer

Data used for alignment: 100k events with more than 3 clusters on SPD

Rate: **0.18 Hz** in agreement with measured flux in the cavern and Monte Carlo simulations

99.6% of events with correct cluster distribution



Cosmic data - alignment

- MillePede2 (global minimization): track-based method to extract the alignment parameters (translations + rotations) of the 2918 ITS modules
- cosmics acquired with SPD trigger: $\sim 10^5$ with $B = 0$, $\sim 10^4$ with $B = \pm 0.5$ T
- alignment done matching top-bottom half tracks

expected spread $\sigma_{\Delta x}^2 = 2 * (r_{SPD2}^2 + r_{SPD1}^2) / (r_{SPD2} - r_{SPD1})^2 * \sigma_{spatial}^2$

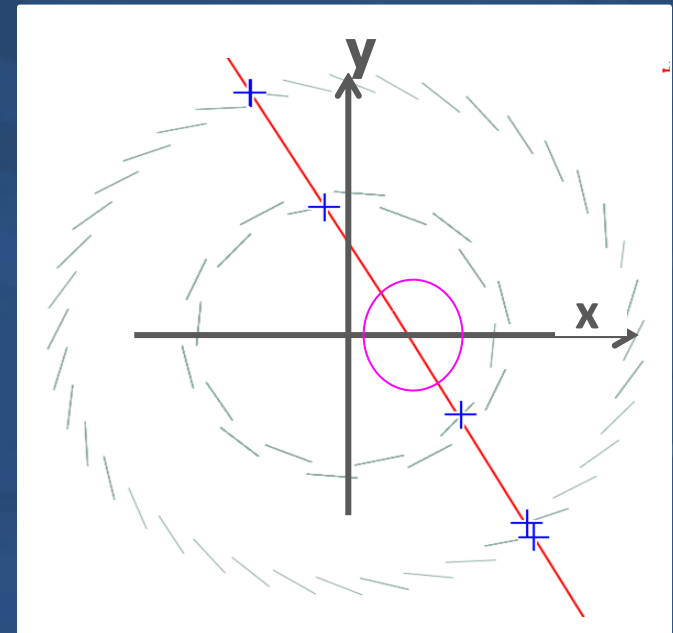
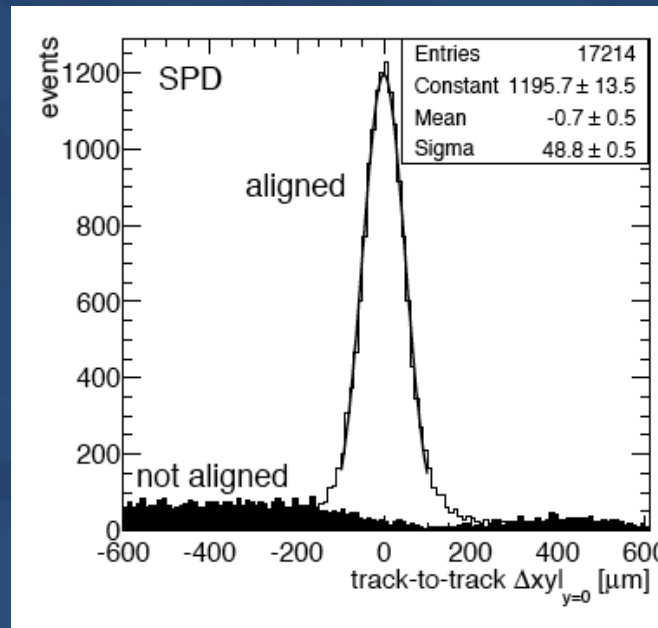
$\sigma = 49 \mu\text{m}$

$\sigma_{spatial} = 13 \mu\text{m}$

$\sigma_{spatial} (sim) = 11 \mu\text{m}$

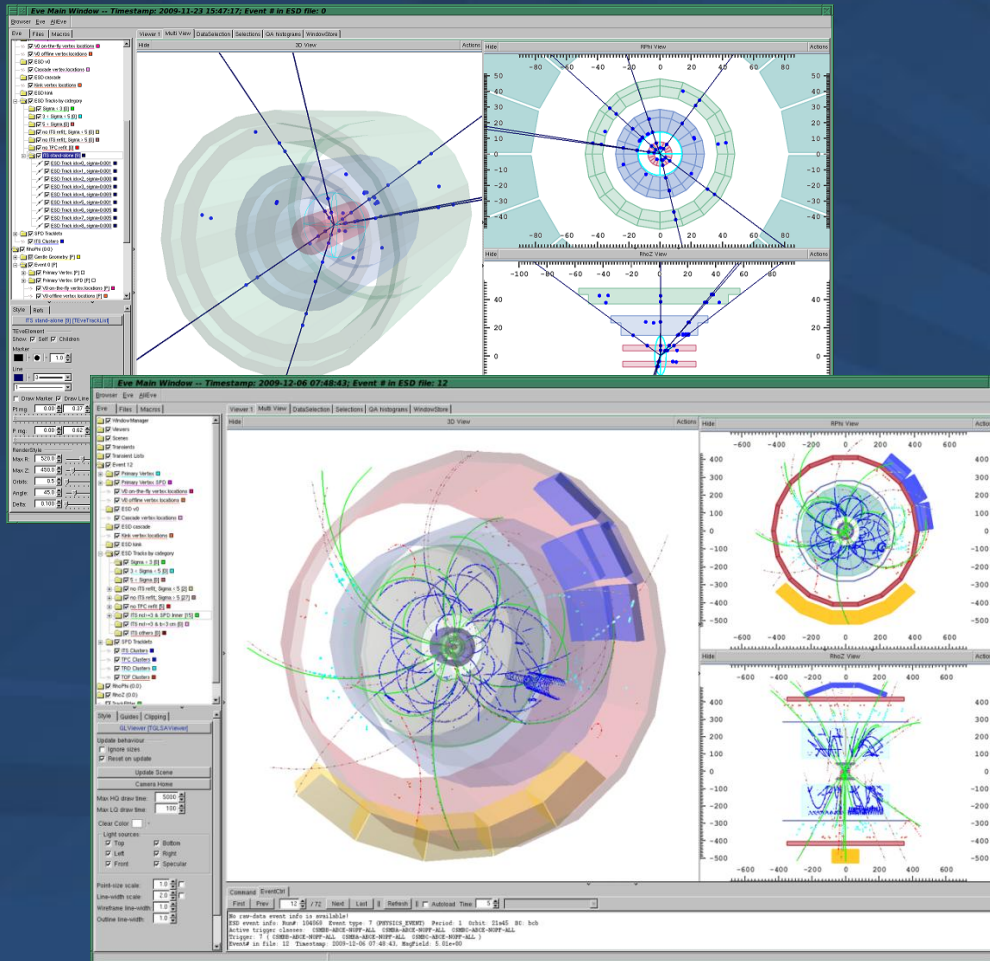


$\sigma_{misal} \approx 7 \mu\text{m}$



Beam data: first collisions

SPD trigger: minimum bias for 900 GeV
minimum bias + multiplicity for 7 TeV



First LHC paper EPJ C: Vol.65, 1 (2010) based on SPD data and trigger

Now preparation for heavy-ion runs:

- configuration to emulate heavy-ion data size (246 kB/event) by lowering readout thresholds
- tests in the laboratory using internal pulser

Summary

First data with beams collected end of 2009

SPD optimization:

- upgrades of the cooling system
- studies on the chip matrix response
- calibration scans on the full detector
- timing studies and adjustments

Fast-OR trigger:

- Fast-OR automatic tuning procedure in place
- trigger efficiencies under study
- timing studies and adjustments

Silicon Pixel Detector & Pixel Trigger are successfully providing L0 trigger for the ALICE experiment

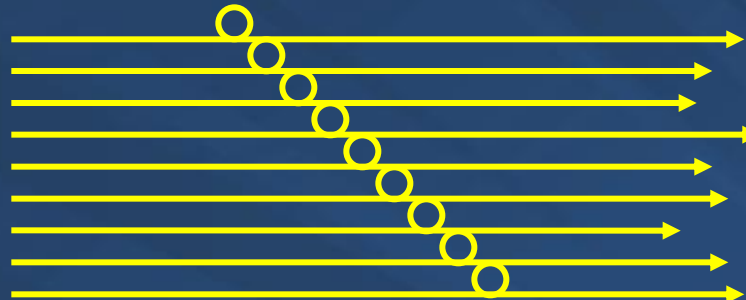
- in cosmic runs
- during injection tests and circulating beams

SPD ready for heavy-ion runs

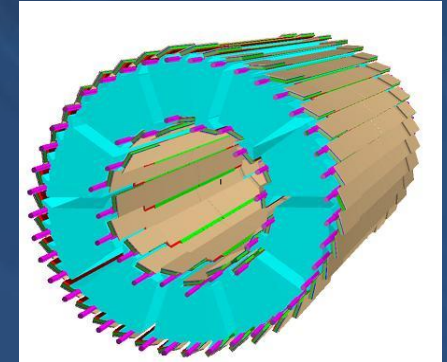
Alignment of SPD clock phases



Clk outputs



Clk fibers (~100m)



Relative phases of 120 clocks of control units:

$$\sigma = 0.63 \text{ ns}$$

Propagation delays due to 120 optical fibers:

$$\sigma = 0.90 \text{ ns}$$

Clock phases at SPD inputs without correction:

$$\sigma = 1.10 \text{ ns}$$

Delays added to the clock transmitters to compensate for differences

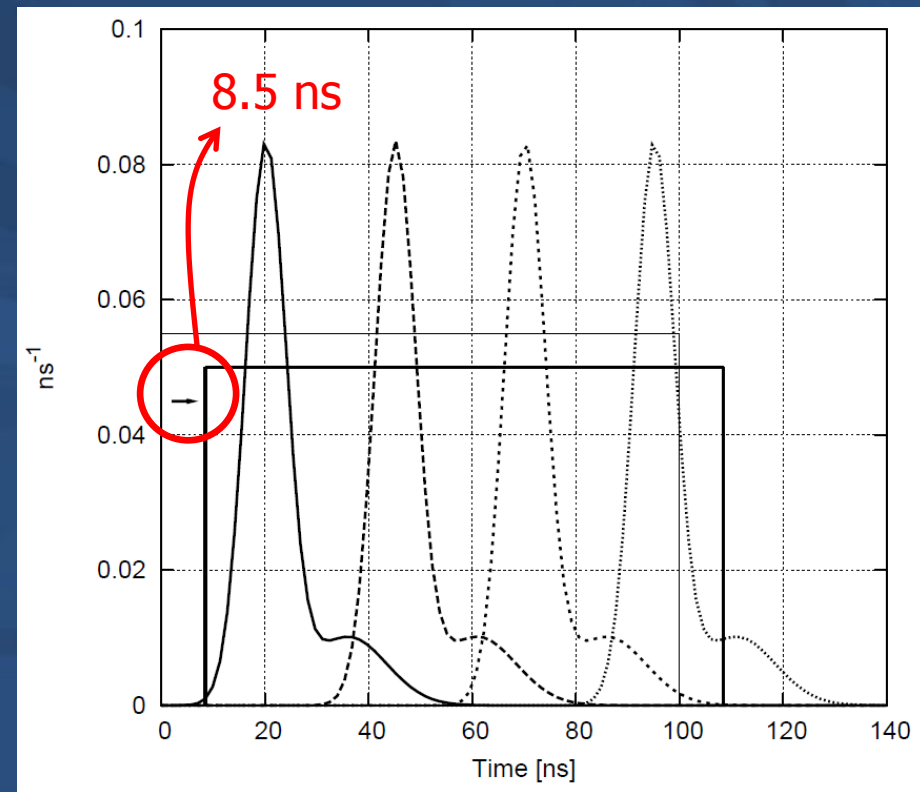
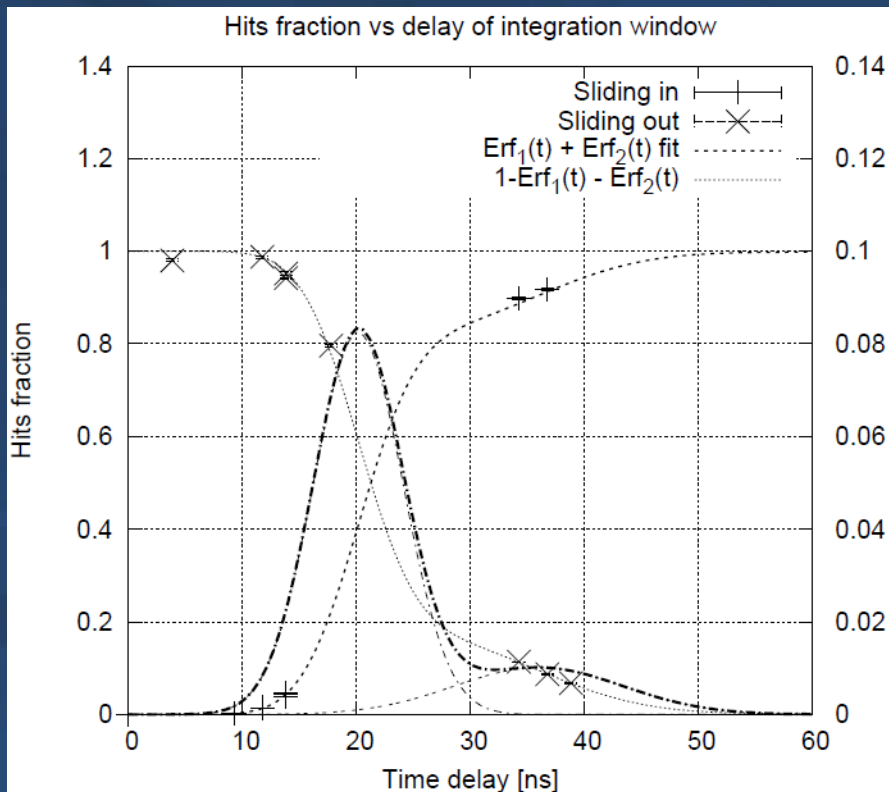
Clock phases at SPD inputs with correction:

$$\sigma = 0.08 \text{ ns}$$

SPD clock fine adjustment

Measure time distribution of average number of hits

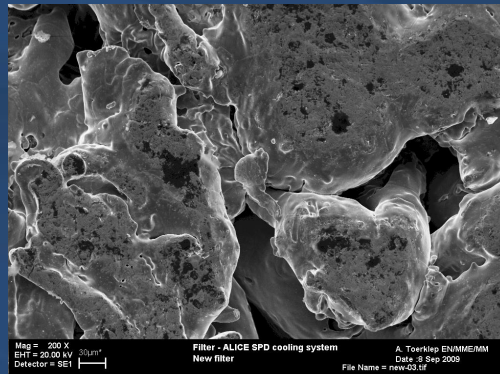
- using 3.5 TeV colliding beams: single phase of colliding BCs wrt SPD clock
- sliding in/out readout strobe window
- changing delay (multiple of clock cycle and fine delay)
- considering average # hits/event



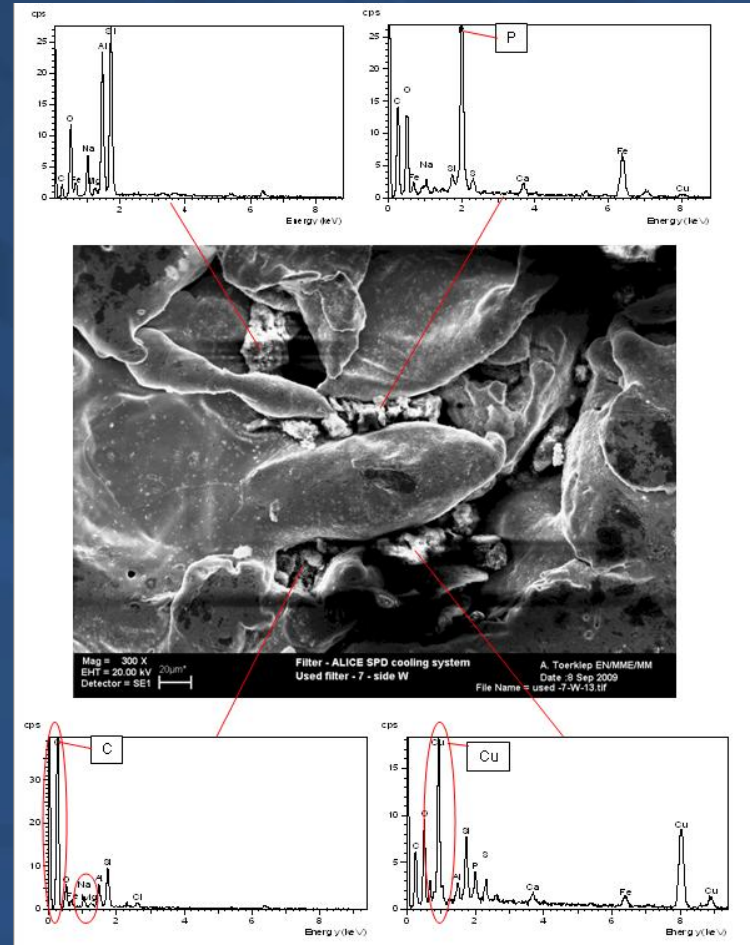
Filters on cooling lines

SEM analysis of microfilters shows clogging, one patch-panel accessible only during long shutdown (need to move TPC)

Clean filter

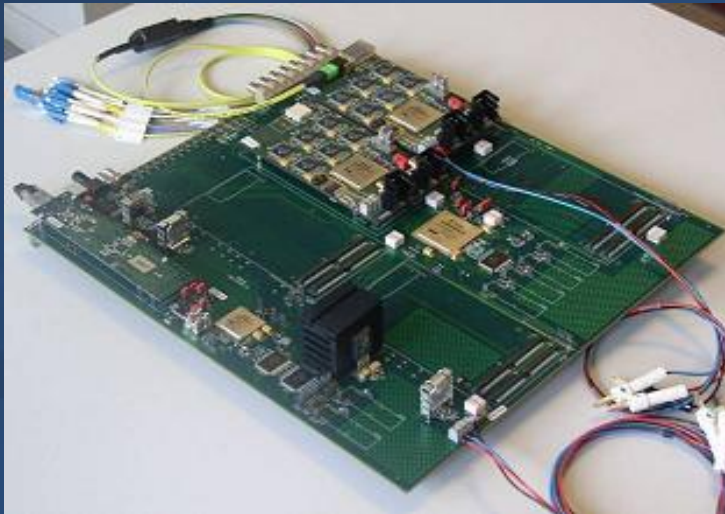


Used filter



Pixel Trigger characteristics

- contributes to the L0 trigger in ALICE
- based on boolean functions (AND/OR) of the 1200 FO bits
- minimum bias + multiplicity trigger for p-p collisions
- centrality trigger for Pb-Pb collisions
- programmable thresholds on inner/outer layers



Output	Algorithm
1	Minimum Bias
2	High Multiplicity 1
3	High Multiplicity 2
4	High Multiplicity 3
5	High Multiplicity 4
6	Past Future Prot
7	Background(0)
8	Background(1)
9	Background(2)
10	Cosmic