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The ALICE Silicon Pixel Detector: commissioning and optimization of the detector performance

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This paper describes the tests and measurements made during the final commissioning of the ALICE Silicon Pixel Detector (SPD) in the first year operation with beams and the optimization of its performance.
The ALICE Silicon Pixel Detector (SPD) is the innermost detector of the ALICE experiment. It consists of two cylindrical layers of pixel detectors, with a total of ~10^7 pixels.
The detector has the unique feature of providing a prompt trigger signal that contributes to the first level trigger decision in ALICE. The trigger signal has been extensively used in the first trigger level of the ALICE experiment, for recording data of proton-proton collisions at energies of 900 GeV, 2.36 TeV and 7 TeV.

Summary

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The ALICE Silicon Pixel Detector (SPD) is the innermost detector of the ALICE experiment. It consists of two cylindrical layers of pixel detectors, with a total of ~10^7 pixels with a size of 50x425 μm2 (rφ x z).
The detector has the unique feature of providing a prompt trigger signal that contributes to the first level trigger decision in ALICE. The trigger is generated from 1200 Fast-OR signals; they are activated by each front-end readout chip and indicate the presence of at least one pixel hit in the chip matrix.

The Pixel Trigger signal has been extensively used in the Level 0 trigger of the ALICE experiment, since the acquisition of cosmic data in 2008-2009 with the aim of integrating all sub-systems and acquiring data for the alignment.
In November 2009, during the LHC start-up, the SPD recorded the first proton-proton collisions in ALICE, and since then the Pixel Trigger has always been used for recording data of proton-proton collisions at energies of 900 GeV, 2.36 TeV and, starting from March 2010, at 7 TeV.

With the data recorded, a strategy for the optimization of the detector performance has been elaborated.
The response of the readout chip matrix has been characterized and optimized. The settings in the front-end chip circuitry have been adjusted to maximize the uniformity of the pixel matrix response.
Dedicated scans were designed and used to find a minimum threshold value that maximizes the signal-to-noise ratio inside the chip circuitry. The new threshold settings were monitored over time and tuned during the detector operation with pp collisions.
The trigger circuitry of each front-end chip needs to be optimized to properly use the SPD as a trigger detector.
The chip settings were tuned in order to maximize the efficiency of the Fast-OR trigger signals and minimize their noise. The correct timing of all the signals coming from the detector was measured, using dedicated functionalities implemented in the off-detector electronics.

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