The TOTEM T1 Read-Out Card motherboard

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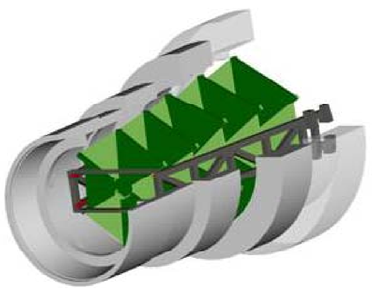
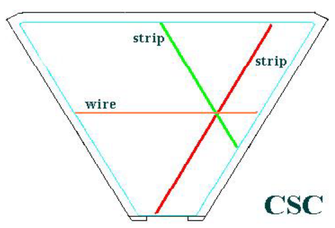
Introduction



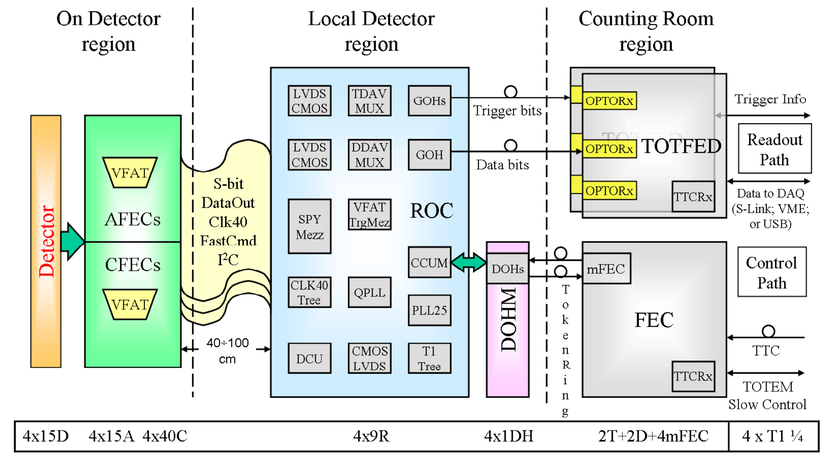
One ARM of T1



The TOTEM experiment is devoted to the measurement of the proton-proton elastic and total cross section at LHC. It is composed of three sub-detectors using different technologies: T1 with Cathode Strip Chambers (CSC), T2 with Gas Electron Multiplier (GEM) and Roman Pots with silicon edgeless microstrip silicon detector. The T1 detector will measure the inelastic rate in the pseudo-rapidity region $3.1 \leq |\eta| \leq 4.7$. The T1 CSC signals from about 11000 anodes (AFECs) and 16000 cathodes (CFECs) are processed and optically transmitted to the counting room via 36 (9 per T1 quarter) T1 Read-Out Card motherboards (ROC). The charge readout of detectors is based on TOTEM front-end ASIC named VFAT, that produces both "Trigger" and "Hit" information. Up to 16 VFATs, mounted on custom hybrids, are connected to each ROC motherboard via flex connections. Next is described the design and functionality of the ROC motherboard and its components as part of the TOTEM T1 front-end electronics system.

Read-out system block diagram

Three logically and physically separated regions define the T1 electronic system architecture. The "***On Detector Region***" where the Front-End ASICs are located, the "***Local Detector Region***" where the data are collected and optically transmitted via the ROCs to the "***Counting Room Region***".



ROC architecture

The TOTEM T1 ROC motherboard is the main component of the T1 front-end electronics system.

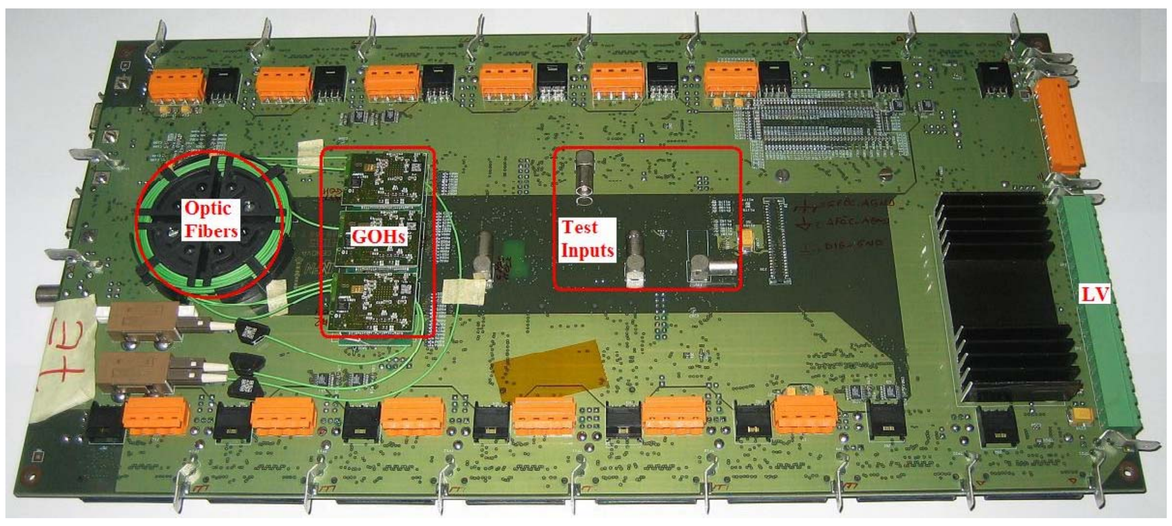
The ROC main objectives are to acquire on-detector data from up 16 hybrids and trigger bits from up 4 out of 16 hybrids (only anodes), to perform data conversion from electrical to optical format and to transfer it to the next level of the system. It also distributes the LHC clock and control information to the hybrids and collect different detector and board parameters.

The ROC accepts several mezzanine modules and contains the following general building blocks:

Data Conversion and Transmission Block – based on LVDS to CMOS converters and Gigabit Optical Hybrid (GOH) module. One GOH module is used to send data from 16 VFAT hybrids to the Counting Room (CR). The GOH transmission, driven by the DAta Valid (DAV) signal generated by the master VFAT, is enabled through MUX circuitry programmable via Slow Control Ring (SCR).

Trigger Transmission Block – based on LVDS to CMOS converters, Trigger VFAT Mezzanine (VTM) and two GOH modules for the optical transmission to the CR. The GOH transmission can be enabled via SCR and sourced by several devices. Trigger GOH synchronization is foreseen via BC0 fast command.

Clock and Commands Distribution Block – based on PLL25 chip, QPLL2 and a number of clocks and commands distribution circuitries. It delivers synchronous clock and commands to every component on the board including the VFAT chips on the FE hybrids. Extracts and distributes the common LHC three bits coded fast command (LV1, BC0, Calib, Resync) from the LHC clock main system, set a programmable latency period (up to 6.4uS) and equalize the clock timing of the anode and cathode hybrids due to the different cables length.



ROC bottom side

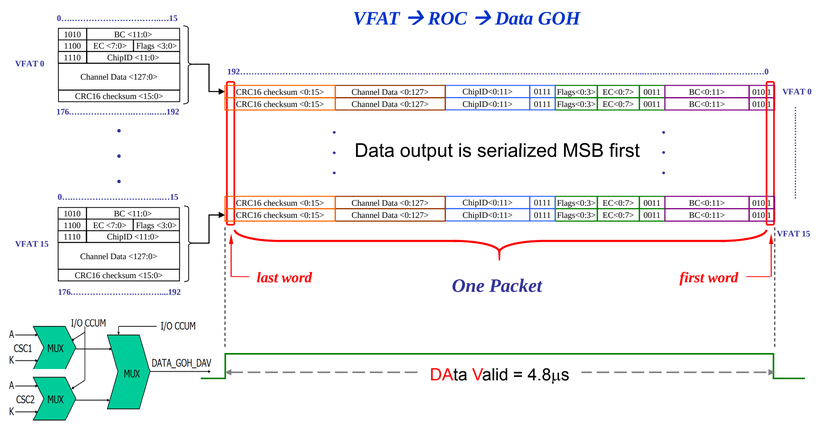
FE inputs and data payload

The ROC motherboard receives both "Trigger" and "Hit" information from the VFAT hybrids.

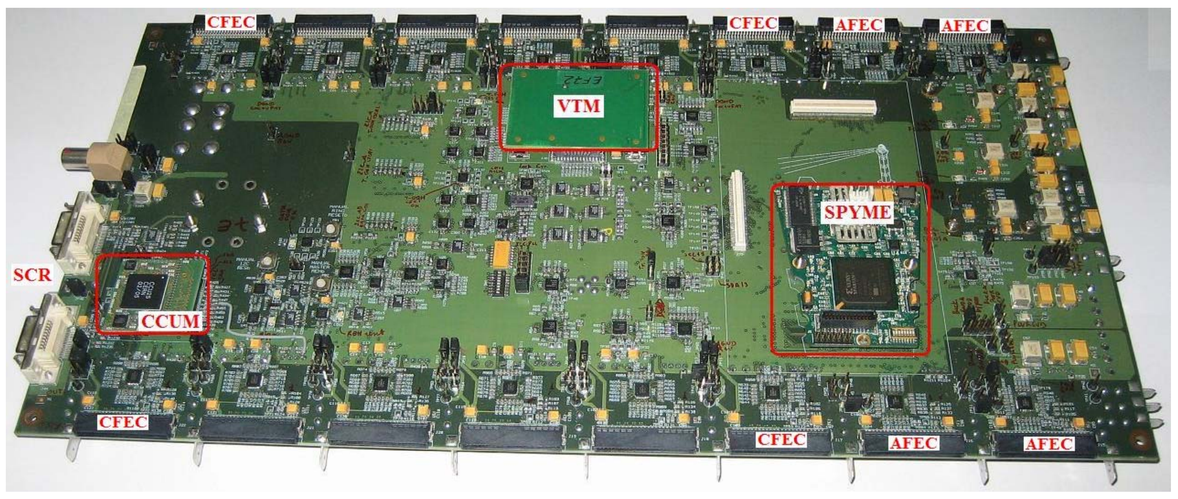
The "Trigger" information in the form of programmable fast "OR", can be used for trigger building.

The "Hit" information is in the form of binary channel data corresponding to a given clock period selected by a first level trigger (LV1A).

On receipt of a trigger (occurring after a given latency period), the corresponding binary data is packaged together with time stamps and other information (i.e. ChipID, CRC) into a 192-bit data packet.



VFAT 192 serial bits → 16VFATs per GOH → 12GOHs per OptoRX and S-Link modules → 192x16x12=36864 bits → ~4kB packet



ROC top side

Control Logic Block – based on CERN common used Communication and Control Unit CCUM mezzanine. This module is connected to the control loop (DOHM and FEC-CCS) via two 20 pins 3M high speed connectors. Control logic block provides 16 I^2C interface channels and one 8 bit bidirectional parallel control port. All the system parameters (i.e. FE hybrid values, clock latency) are sent to the devices via I^2C, while GOHs power cycle, GOHs status, Data and Trigger GOH sources, Soft and Hard Reset are managed via the parallel port. A skip fault architecture for additional redundancy based on the doubling of signal paths and bypassing of interconnection lines between CCUM is also implemented.

Auxiliary Debugging Block – based on a FPGA programmable custom mezzanine (SPYME). This module emulates the DAQ system located in the CR and remotely can tests all the ROC functionalities via USB 2.0 connection provided on it.

LV Distribution Block – based on independent PCB layers strategy for analog and digital low voltages distribution. The ROC provide power to the 16 VFAT hybrids, to the Slow Control Ring based on CCUM module and all other circuitries. Regulators radiation tolerant are also foreseen.

Conclusions

The TOTEM T1 ROC motherboard is fully integrated within the TOTEM DAQ and also fully compatible with CMS DAQ requirements. Prototypes have proven to comply with the required functionalities and performances. The complete set of boards (36) necessary to equip the T1 detector have been built, tested and are already mounted on the detector.