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The Front-end Electronics of the LHCb Upgrade

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The LHCb detector and its electronics architecture are optimized for the measurement of b-physics at LHC. The current detector is complete and taking data, and will run at a luminosity of 2 x 10^32 cm-2s-1 to collect around 6fb-1. It is expected to reach this target around 2016 and hence a programme is already underway towards an upgrade of the detector and its electronics systems at this time. The aim of this upgrade is to allow a large statistical improvement in the data as well as a search for new physics by running at an increased luminosity of 2 x 10^33 cm-2s-1. This increase is only advantageous if certain limitations imposed by the existing electronics architecture are removed. Hence a new architecture has been developed, a specific feature of which is the requirement that all detectors process and transmit data from every LHC bunch crossing. Triggering is then done in a high-performance farm of CPUs. This paper will describe the architecture and review the status of the development work underway in all the sub-detectors, with focus on those sub-systems unique to LHCb.

Summary

The LHCb detector has been constructed with the specific aim of measuring b-physics at the CERN Large Hadron Collider (LHC). The layout of the experiment and its sub-detectors has been optimized to measure the products of proton-proton interactions within an acceptance of ±300mrad about the beam axis, where the majority of b-hadrons will be produced. Data from these detectors are read out by a front-end electronics system that has also been designed to maximize the efficiency of LHCb at a target luminosity of 2 x 10^32 cm-2s-1. When an integrated luminosity of 6fb-1 has been reached, LHCb will then upgrade and run at a luminosity of 2 x 10^33 cm-2s-1. Any luminosity increase, however, can only be exploited if limits imposed by the existing Level-0 hardware trigger are removed. This requires a new electronics architecture, the main feature of which is the transmission of detector data from every LHC bunch-crossing to a farm of CPUs where complex triggering algorithms will be implemented. This allows a very flexible and powerful trigger, a feature that is expected to be essential in future b-physics programmes. However, this requires that all sub-detectors will have to modify or change completely their front-end electronics to transmit data from the bunch crossings at 40MHz.

LHCb is planning an efficient upgrade in terms of total cost and development and installation time. This implies the re-use of existing electronics and infrastructure as much as possible. Some systems, such as the Outer Tracker and Muon detectors, are modular enough that they can re-use their current analog electronics. Other systems, such as the Vertex Locator and Ring-Imaging-Cherenkov detector, will require a complete re-design of the electronics. Here, custom developments are being actively pursued in collaboration with other projects. New front-end ASICs are under design, and the advantages of 130nm CMOS in terms of power consumption and density are proving beneficial. All of the detectors will change their data transmission systems to make use of the Gigabit-Transceiver and Versatile-Link components under development for the LHC experiment upgrades. Much of the effort is concentrated on minimizing the number of these links by implementing data-compression algorithms on the front-end modules. To this end, tests are underway to evaluate the potential use of commercial programmable devices in the relatively modest radiation environment of LHCb. These offer advantages of development cost and flexibility over ASICs, and are being considered by many sub-detectors. The data bandwidth expected from the detector is about 35 Tbit/s, and this will be transmitted to common readout boards, known as TELL40, that interface the front-end electronics to the data-acquisition (DAQ). Included on the TELL40 will be a data throttling mechanism to allow recovery from buffer overflows. It also permits a possible staging of the DAQ where the system would be gradually built up to finally accept the full 40MHz data. This throttle can also include physics information from the Calorimeter and Muon systems.

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