Topical Workshop on Electronics for Particle Physics 2010 — Aachen, Germany, 20-24 September, 2010

Subnano Time to Digital Converter implemented in PARISROC for PMm² R&D program

http://pmm2.in2p3.fr

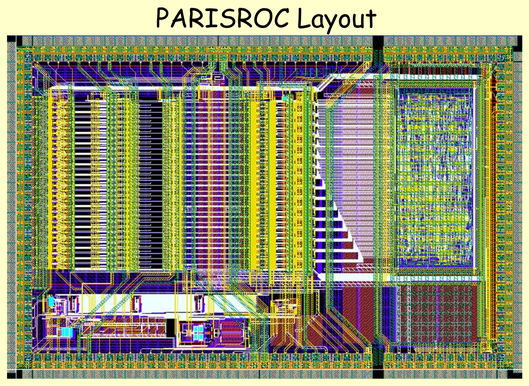
S. Drouet on behalf of the PMm² collaboration

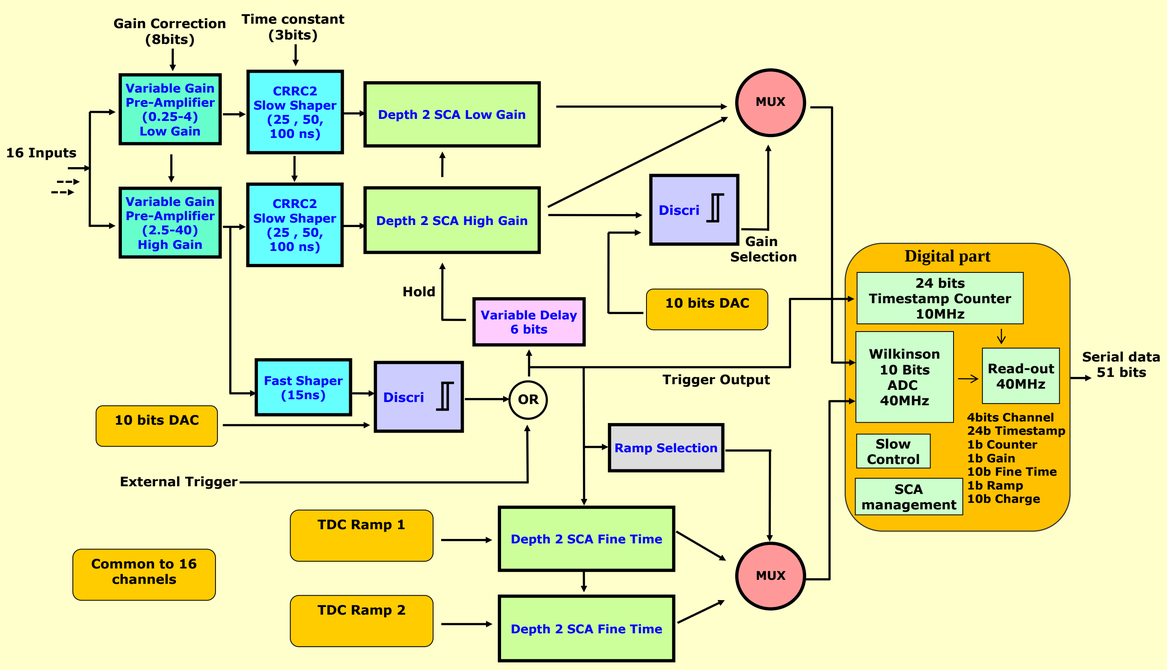
PARISROC

PARISROC_v2 is a dedicated front-end ASIC for photomultiplier tubes designed by LAL/OMEGA group and by IPNO for the analog TDC.

- AMS SiGe 0.35µm, size: 5 mm x 3.4 mm
- 16 independent channels
- Independent gain adjustment by channel
- Charge and time digitization
- Serial readout @ 40 MHz
- Charge: 0 to 300x10⁶ electrons
- Efficiency from 10⁶ e⁻ input charge
- Virtual 12-bit ADC @ 40 MHz (10-bit Wilkinson ADC + 2 gains with automatic selection)
- Time measurement:
  - Analog TDC: Dyn. = 100 ns, step 220 ps, resolution 425 ps RMS
  - Digital TDC: Dyn. = 1.67 s, step 100 ns (24 bits / 10 MHz)

PARISROC Layout

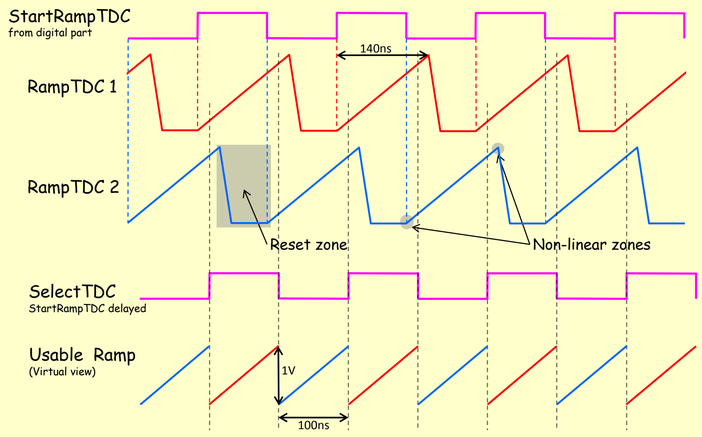




Synoptic of PARISROC ASIC

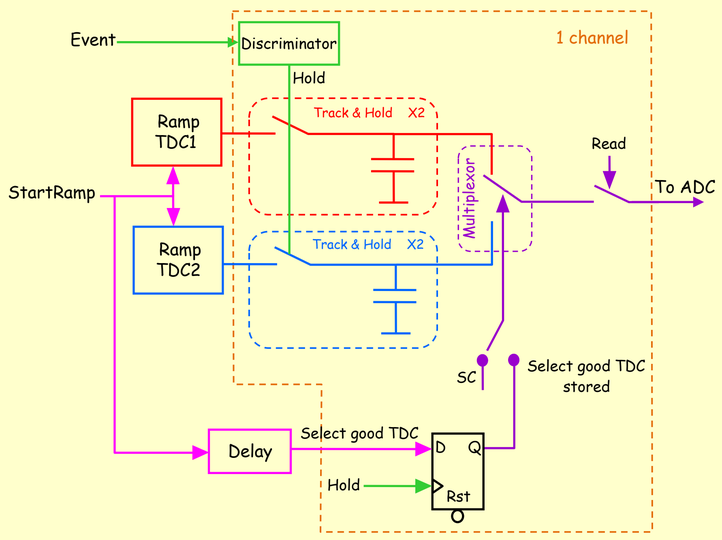
Analog TDC Principle

2 ramps working in phase opposition with overlap zones. When one is in the reset zone, the other is in the linear zone. Therefore, the time measurement is possible without blind zone because, at least, always one of the two ramps is in a linear zone. A digital module, implemented in each channel, selects the valid TDC ramp.



Functionnal Chronograms

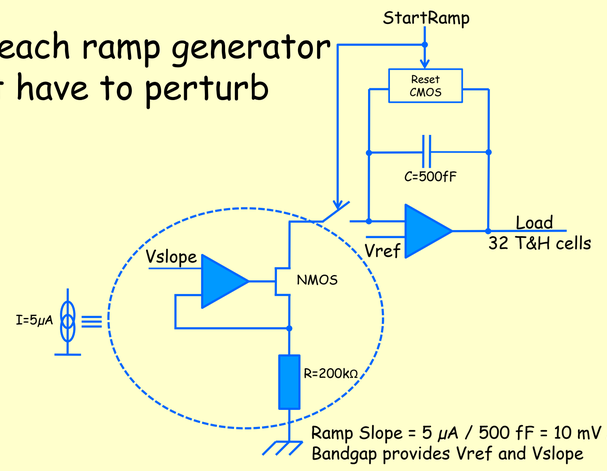
When an event occurs, the 2 ramps are sampled at the same time in the Track&Hold cells and a logic module tags the valid one. Only the sample of the selected ramp is converted.



Principle

TDC Ramp Generator

- Architecture: a simple current source and an integrator.
- Loads: 16 channels ➔ 32 T&H cells with independent switching (1 T&H = 500 fF)
- Load variation: from 0 to 16 pF on each ramp generator
- Constraint: Charge variation do not have to perturb the linear zone of a ramp
- Ramp Slope: 10 mV / ns
- Ramp Dynamic: 1.4 V / 140 ns
- Usable Ramp Dynamic: 1 V / 100 ns
- Target resolution: 100 ps



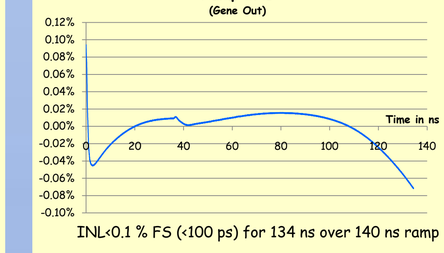
One Ramp Generator Schema

Special Cares

Design:

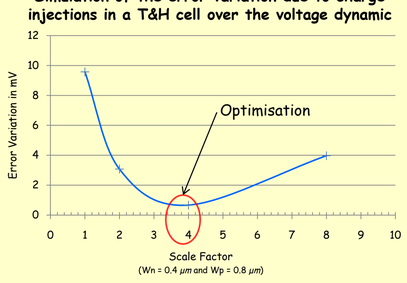
- Ramp generator linearity
- Charge injection in memory cells: Optimization of switch sizes
- Immunity of a cell relative to switching neighbour cells

Ramp INL (Gene Out)

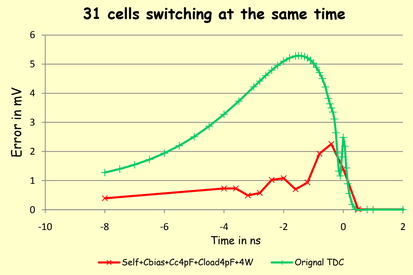


INL<0.1 % FS (<100 ps) for 134 ns over 140 ns ramp

Simulation of the error variation due to charge injections in a T&H cell over the voltage dynamic



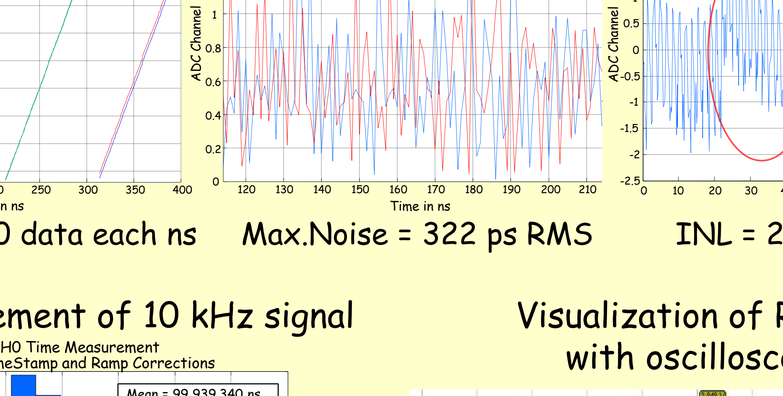
Memorization error in a referred cell with 31 cells switching at the same time



Layout:

- Centroid layout for the amplifier input pairs
- Mirroring of the 2 TDC ramp generators
- Dedicated power supplies

The goal of these special cares is to minimize mismatching and obtain the same charateristics on each ramp. And as the ramps work in opposition phase, the reset zone of one ramp must have the lowest possible impact on the other.



Dual-Ramp Generator Layout

Tests and Results

Ramps reconstruction, noise and INL measurements:

Mean of 10 000 data each ns

Max.Noise = 322 ps RMS

INL = 2 ch ➔ 450 ps

Time measurement of 10 kHz signal

Visualization of Ramps with oscilloscope

IPN Orsay: IN2P3-CNRS-Université Paris Sud 11
http://ipnweb.in2p3.fr
S. Drouet, B. Genolini, B.Y. Ky, T. Nguyen Trung, J. Peyré, J. Pouthas, P. Rosier, E.Wanlin

LAL Orsay: IN2P3-CNRS-Université Paris Sud 11
http://www.lal.in2p3.fr
J.-E. Campagne, S. Conforti, F. Dulucq, M. El Berni C. de La Taille, G. Martin-Chassard

LAPP Annecy: IN2P3-CNRS-Université de Haute Savoie
http://lappweb.in2p3.fr
D. Duchesneau, N. Dumont-Dayot, J. Favier, R. Hermel, J. Tassan-Viol, A. Zghiche

Université Libre de Bruxelles
http://www.ulb.ac.be
K. Hanson

ANR-06-BLAN-0186