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Subnano Time to Digital Converter implemented in PARISROC_V2 for PMm² R&D program

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PARISROC_V2 is a complete read out chip, in AMS SiGe 0.35µm technology, for photomultipliers array. It allows triggerless acquisition for next generation neutrino experiments and its belongs to an R&D program funded by the French national agency for research (ANR) called PMm²: "Innovative Electronics for photodetectors array used in High Energy Physics and Astroparticles". The ASIC integrates 16 independent and auto triggered channels with variable gain and provides charge and time measurement by a 10-bit Wilkinson ADC and a 24-bit counter. The time measurement is made by 2 complementary systems: a 24-bit gray counter (coarse time) with a step of 100ns, and a double ramp TDC (fine time) with a 10-bit resolution and a precision less than 1 ns. It is interesting to underline the fact that the double ramp generator is common to all channels. The poster presents the TDC architecture and the first fine time measurements.

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