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ABSTRACT
The pixel detector of the CMS experiment at the LHC is read out by analog optical links, sending the data to 9U VME Front-End Driver (FED) boards located in the electronics cavern. There are plans for the phase 1 upgrade of the pixel detector (2016) to add one more layer, while significantly cutting down the overall material

budget. At the same time, the optical data transmission will be replaced by a serialized digital scheme. A plug-in board solution with a high-speed digital optical receiver has been developed for the Pixel FED readout boards and will be presented along with first tests of the future optical link.

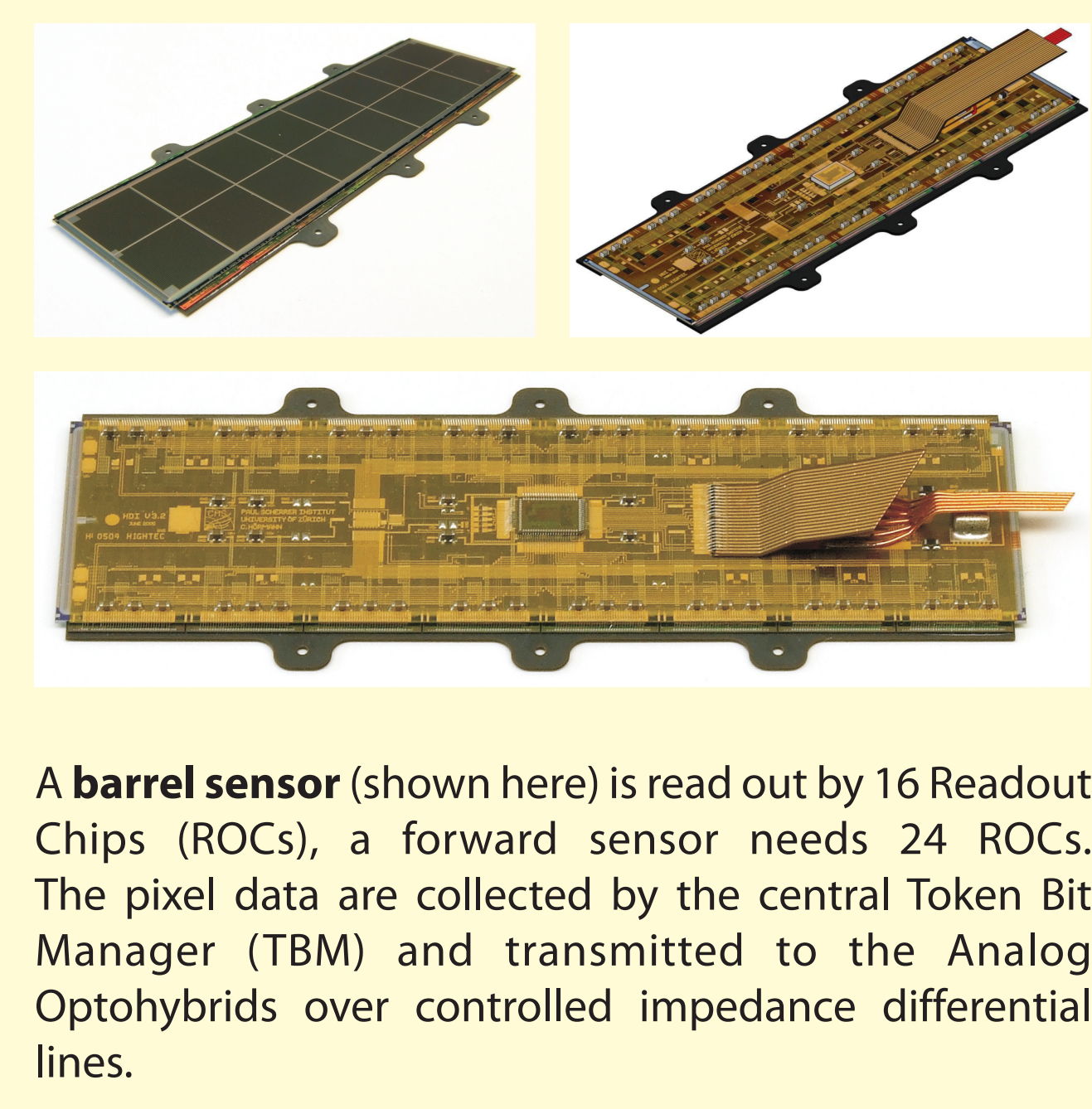
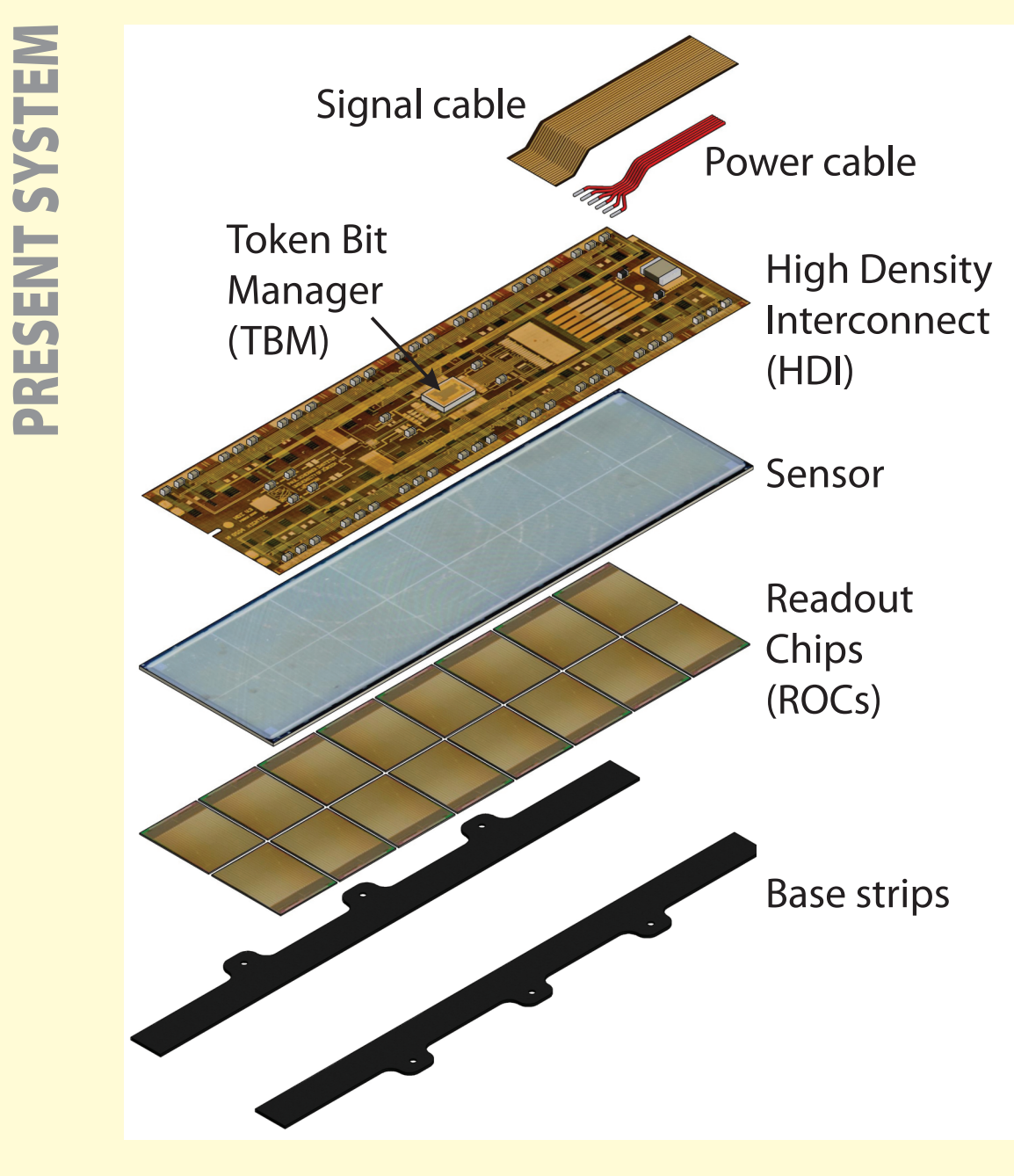
DETECTOR GEOMETRY

3 barrel layers
r = 4.4 / 7.3 / 10.2 cm
48 million pixels
0.78 m² sensitive area

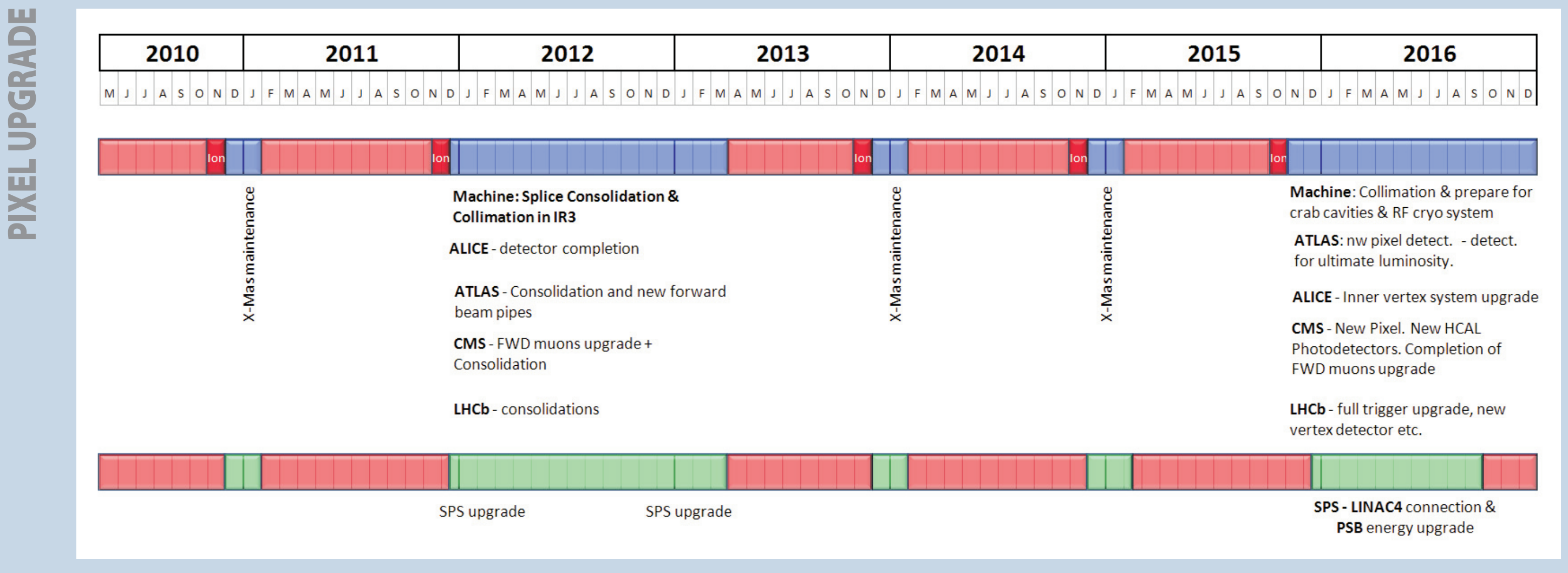
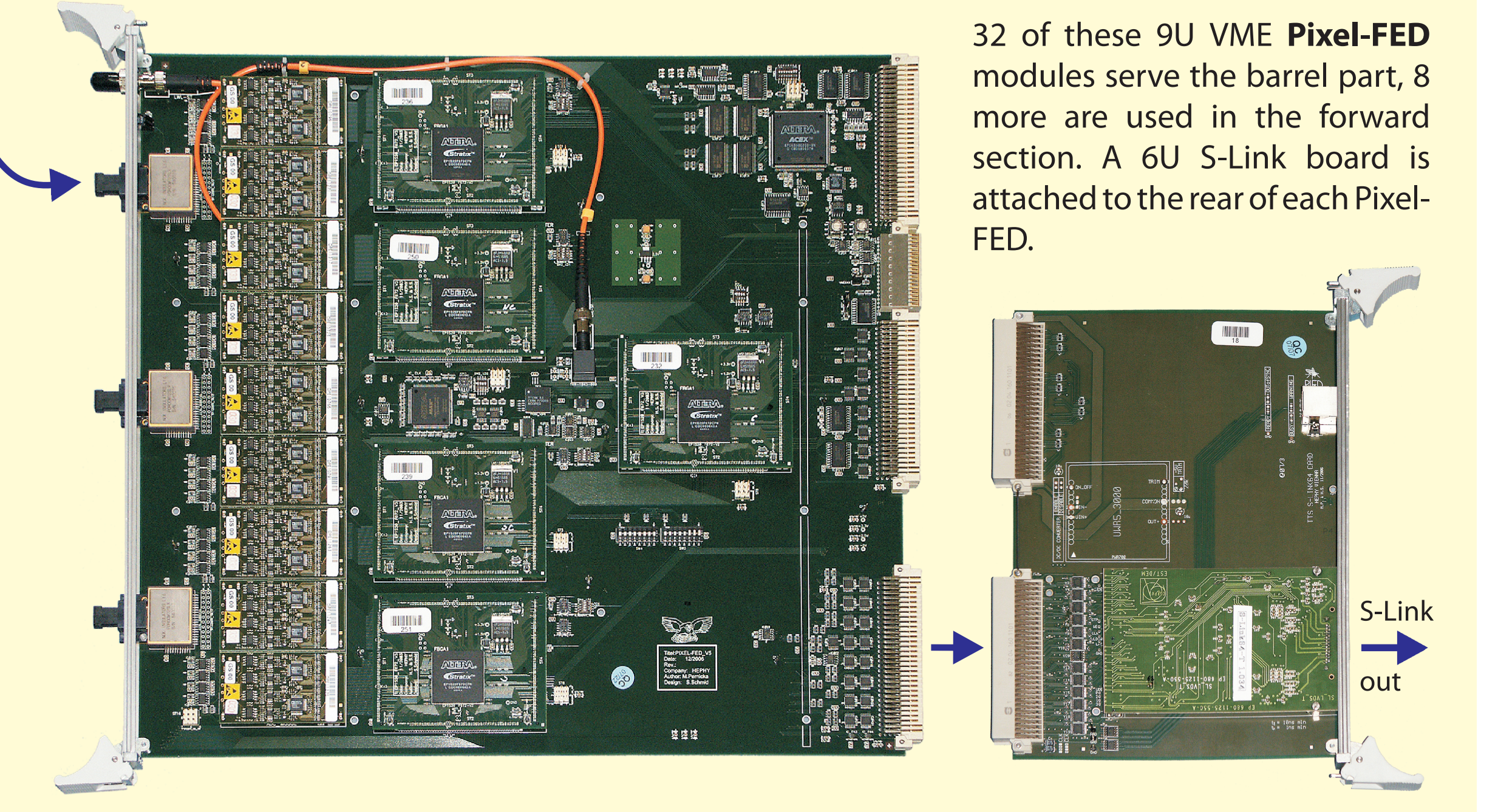
2 forward discs (per side)
18 million pixels
0.28 m² sensitive area

READOUT CHIP

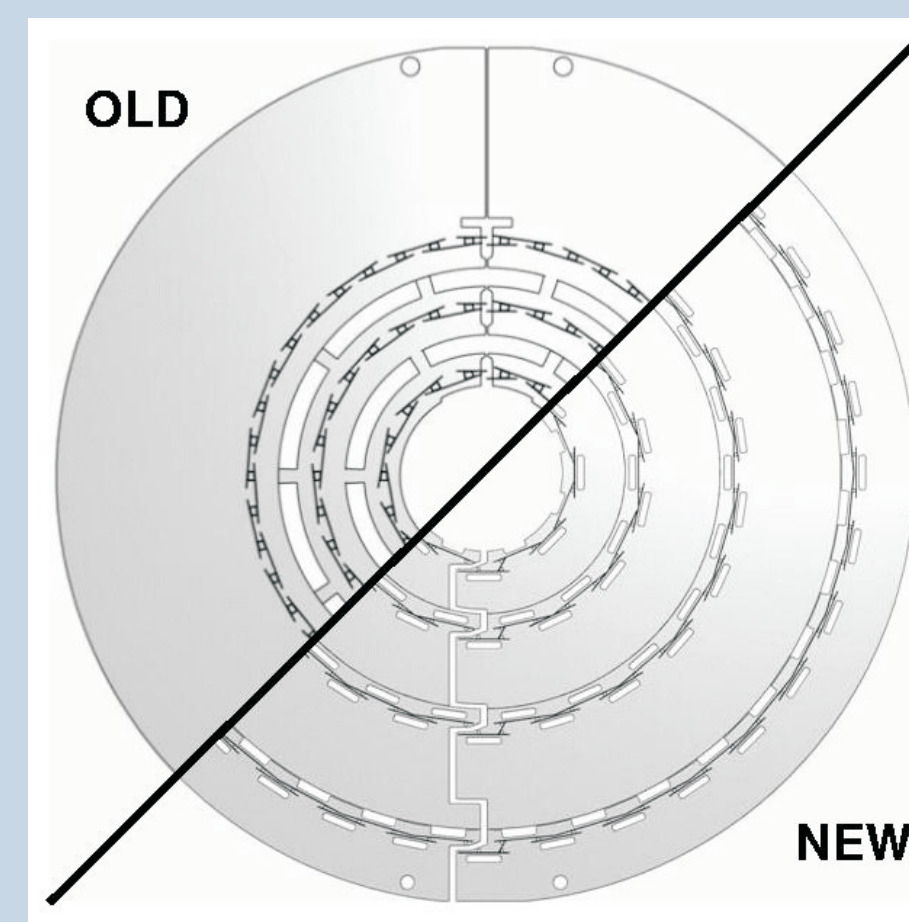
52 x 80 = 4160 pixels
9.8 x 7.9 mm² size
0.25 μm CMOS



The pixel hit data are converted to optical signals using **Analog Optohybrids** which are composed of six laser diodes. One Optohybrid (6 channels) serves 3 sensor modules.



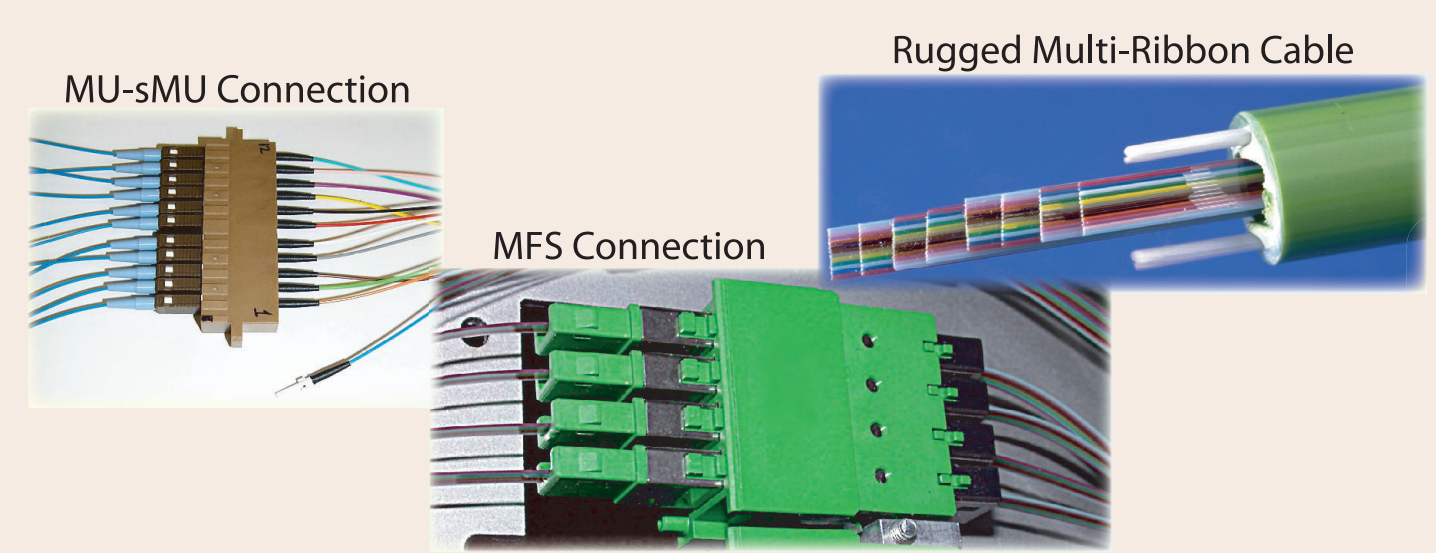
The year 2016 is dedicated to maintenance, which includes the installation of a new pixel detector in CMS.



	OLD	NEW
Barrel Layers	3	4
Forward Discs (per side)	2	3
Total Weight [kg]	3.99	1.72

Even though the future pixel detector will be considerably larger than the present one, it will also have a significantly reduced material budget thanks to the application of **carbon fiber** compound materials and **CO₂ cooling**.

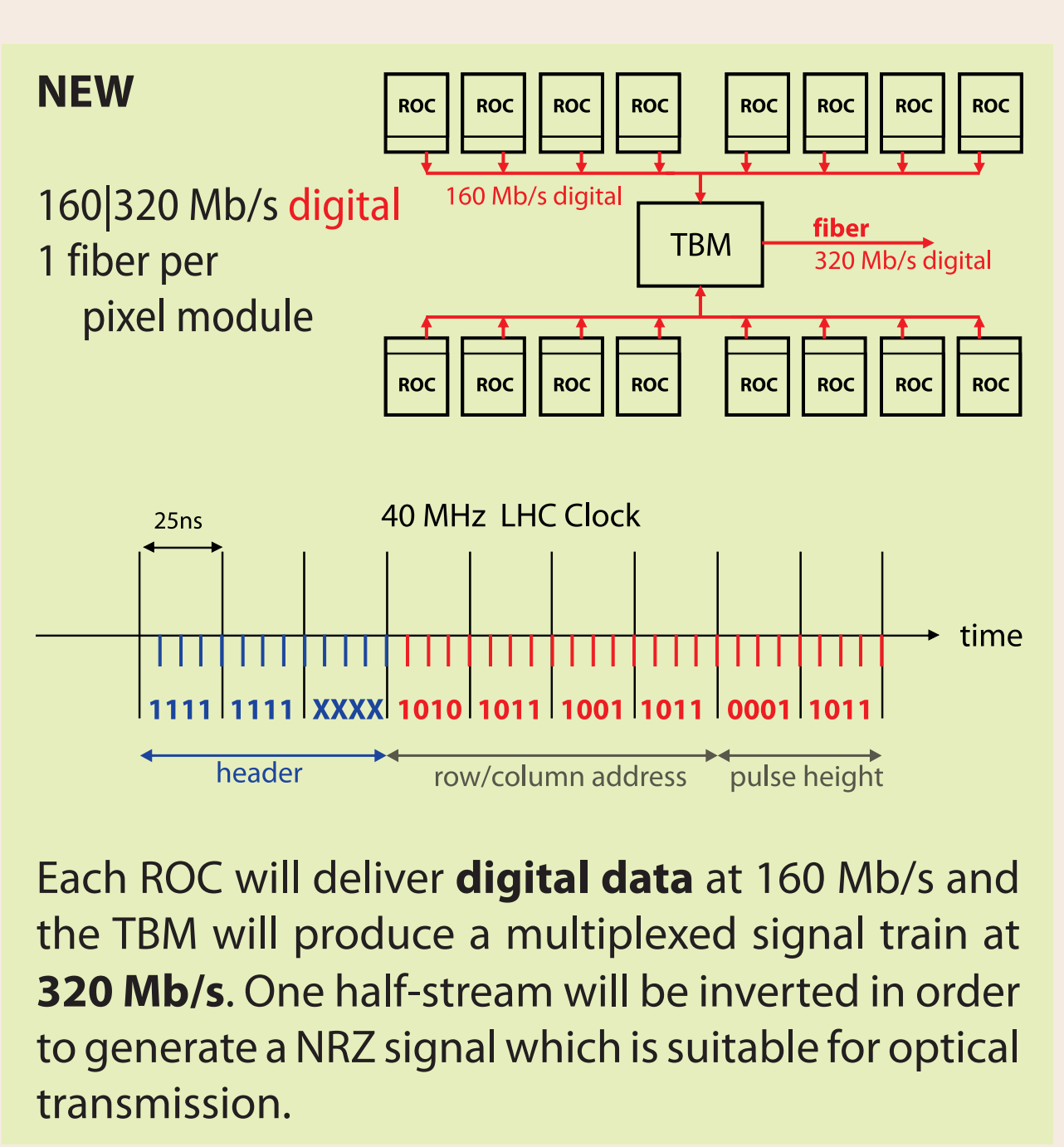
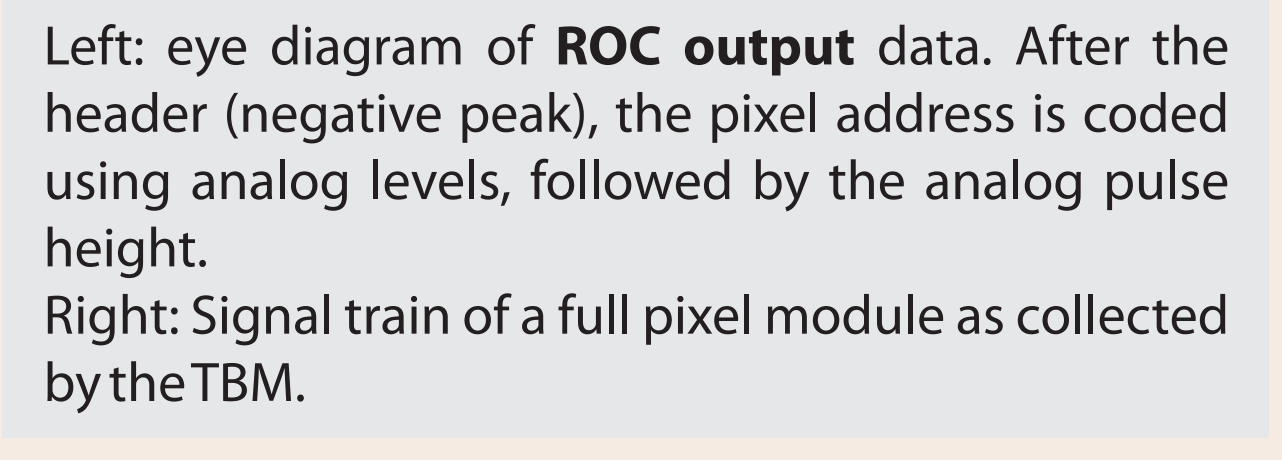
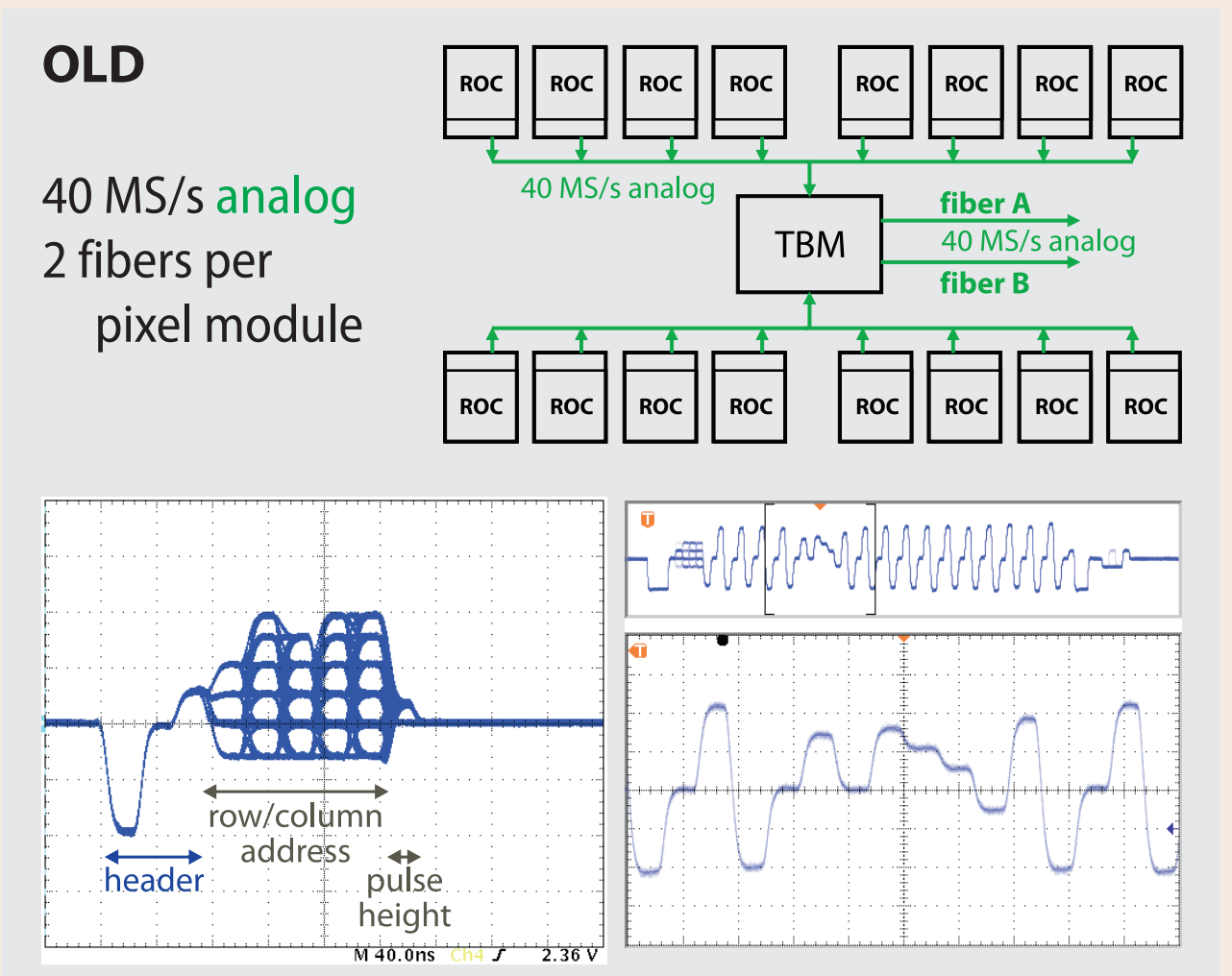
FUTURE READOUT
The Pixel Detector is read out by **optical fibers**, running from the innermost part of the CMS experiment to the adjacent electronics cavern. The upgrade must be done under the assumption that **only existing fibers can be re-used**, but no additional ones are installed. This implies that the data throughput of each fiber must increase. Presently, each pixel module is read out by 2 optical fibers. In the future, only one line will be available, apparently at twice the data rate.



MODIFICATIONS
Clearly, the new readout scheme requires changes in several devices.

ROC	Minor changes in output circuitry (PLL and serializer instead of DAC)
TBM	New chip (fully digital instead of analog)
Optohybrid	Faster digital device (bandwidth of present one is marginal)
Fiber	Unchanged → defines constraint: Single-mode 1310nm
Receiver	Faster digital device (bandwidth of present one is too low)

The receiver is located on the Pixel-FED. First tests with a suitable device are shown on the right side of this poster.



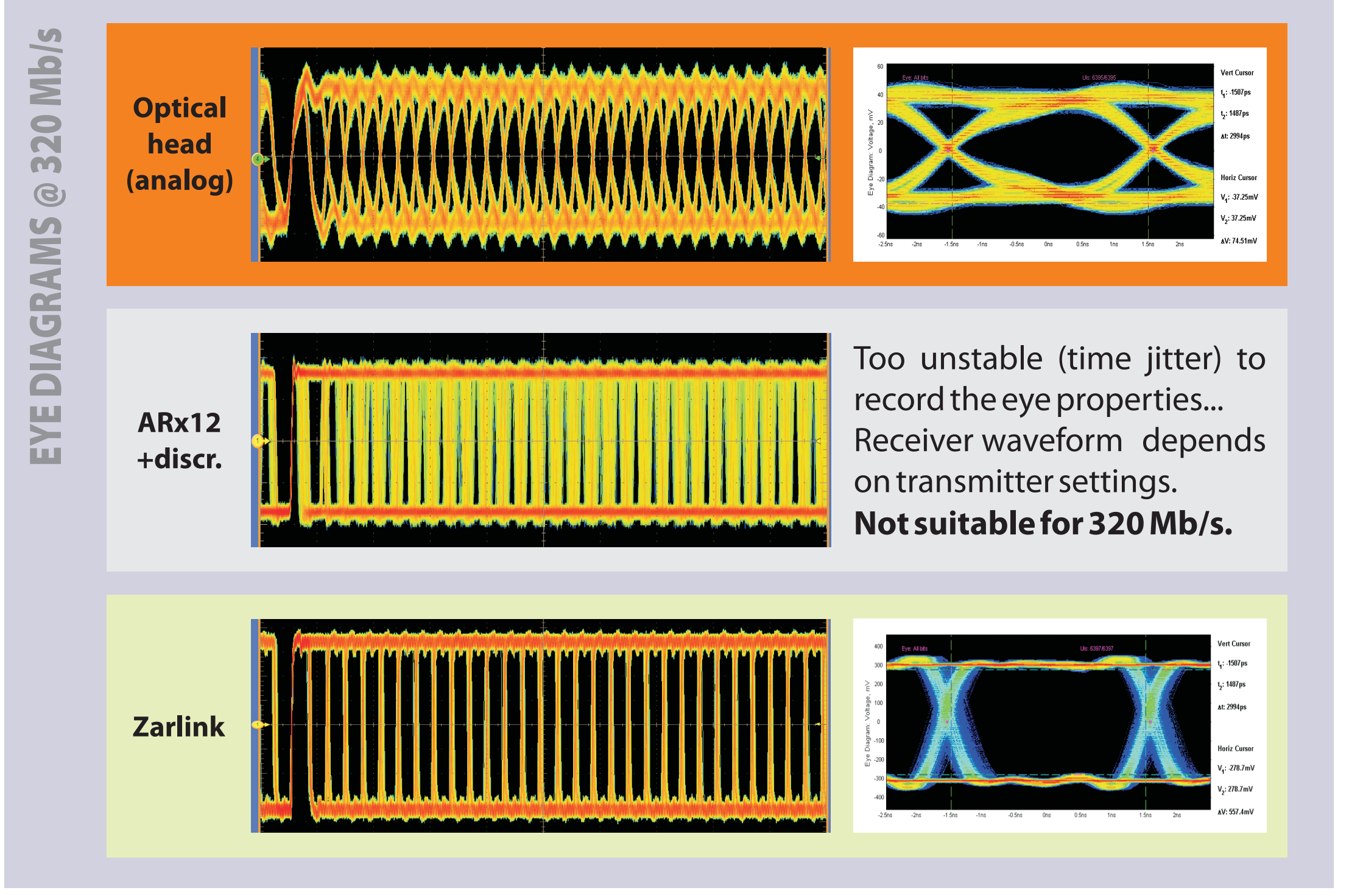
TEST OF NEW RECEIVER

Unfortunately, most **commercial** optoelectronics operates in the **near infrared** regime. However, due to the fiber constraint, we require operation at **1310nm**. Moreover, the ideal receiver would feature a 12-way **MPO fiber connector**, which then would be a direct replacement of the existing analog receivers. Such a device does not exist on the market, but **Zarlink** (now Tyco) provided engineering samples of a modified standard device, which was tested for application in the Pixel-FED.

Agilent 8110A pulse/pattern generator
Analog Optohybrid (3-laser variant)
Zarlink receiver
ARx12 receiver (with discriminator)
Optical head

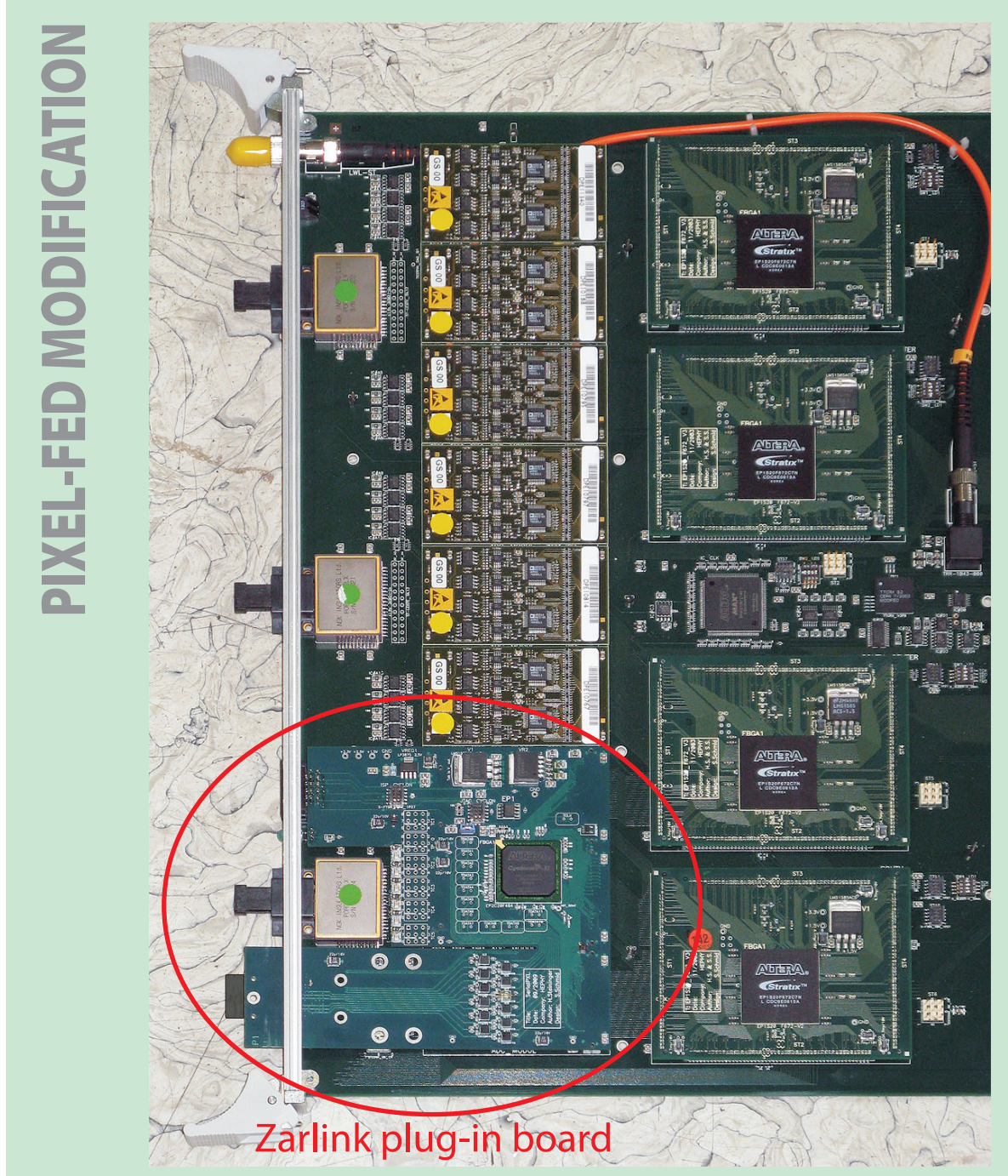
OLD (analog)
NGK ARx12
12 x 100 MHz

NEW (digital)
Zarlink ZL60110
12 x 2.7 Gb/s

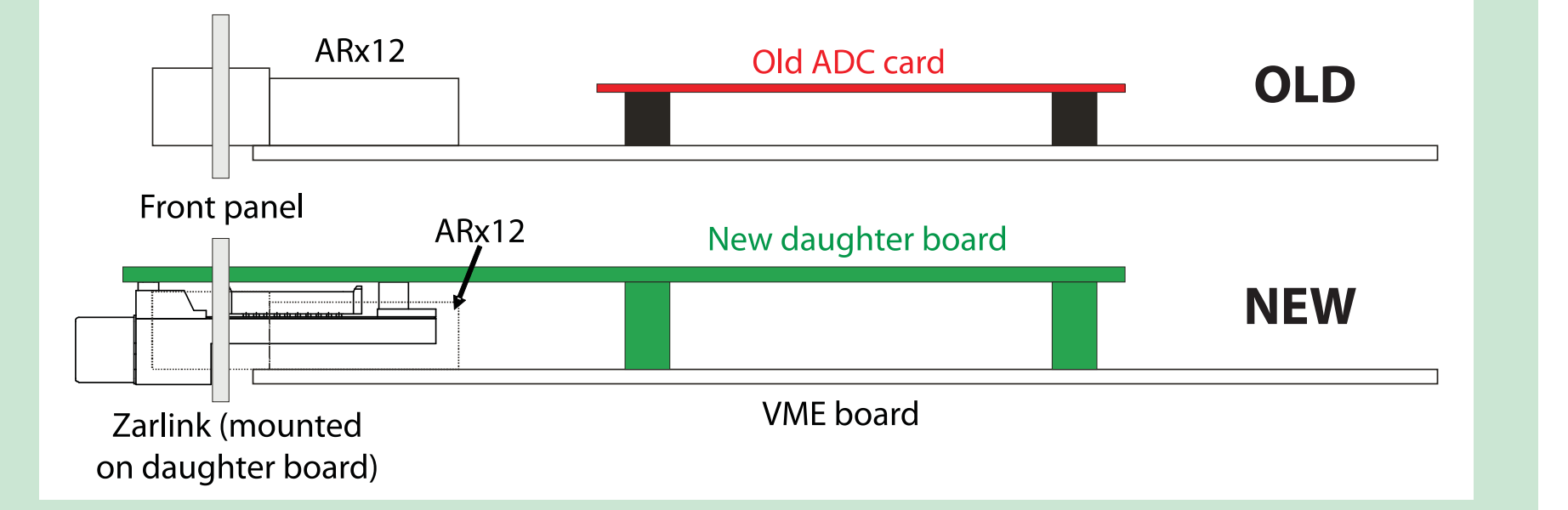


NRZ TESTS

Heavily **unbalanced code** (here: 1000 0000 = 12.5% duty cycle) is correctly identified by the optical head (top), but not by the Zarlink receiver (bottom). However, **temporary excursions** – up to 700 consecutive 0s or 1s – from an otherwise balanced code are **well tolerated** by the Zarlink receiver.



The present Pixel-FED contains three 12-way analog receivers and 3 x 3=9 ADC daughter boards. Obviously, neither analog receiver nor ADCs are needed anymore when going digital, while it would be economical to **retain all the other parts** of the Pixel-FED. Under these premises, we devised a plug-in board that replaces 3 adjacent ADC boards. It contains the **Zarlink** optical receiver and an **FPGA for deserialization**. Eventually, the data is passed on to the existing subsequent stages in a parallel fashion. With this solution, the existing analog receivers does not have to be unsoldered from the Pixel-FED, which allows to **easily switch** between old and new hardware.



DESERIALIZATION
As the pixel data do not follow any standard protocol, we cannot make use of existing FPGA solutions. In particular, the **synchronization** to the serial data stream is tricky. This work was started and is in progress... Our approach is to sample the incoming serial data with several different clock phases (this essentially corresponds to **oversampling**), **histogram the transitions** between adjacent samples and pick the clock phase with **maximum distance to transitions**.