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The GBT-Serdes ASIC prototype: test features and preliminary results

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In the framework of the GigaBit Transceiver project (GBT), a prototype of the GBT-SERDES ASIC has been developed. In charge of the serialization-deserialization of the data, including Reed-Solomon encoding, clock recovery, precise PLLs and complex frame-alignment procedure, this chip has been designed in a commercial 130nm CMOS technology to sustain high radiation doses and operate at 4.8 Gb/s. The first wafer of these chips arrived at the end of May 2010. In this paper, we present the GBT prototype chip, his testing features, the system designed to fully qualify the component and the preliminary results obtained.

Summary

In the framework of the GigaBit Transceiver project (GBT), a prototype of the GBT-SERDES ASIC has been developed. This chip is in charge of the serialization-deserialization of data, operating at 4.8 Gb/s. Unlike the final GBT which will be equipped with e-ports to deal with the parallel I/Os, the parallel ports of this prototype are based on busses of 30-bits running at 160MHz, four of those frames making a full 120-bits frame running at 40MHz. This chip also includes a robust encoding/decoding system based on the Reed-Solomon scheme. The deserializer part contains a circuit in charge of clock recovery, precise PLLs and a complex frame-alignment state machine. This chip has been designed in a commercial 130nm CMOS technology to sustain high radiation doses and operate at 4.8 Gb/s. To fully qualify the behavior of each block in the component, many tuning registers have been implemented. In particular, several types of clock recovery techniques will be tested within the chip. The delicate frame alignment circuit can as well be adjusted with many parameters. Of course, the GBT can also be partially tested, focusing on each critical step by using internal loopbacks. A GBT tester board has also been designed and produced with various types of layers stack-ups to allow a good understanding of constraints that the GBT would possibly impose to PCBs. The full tester includes an evaluation kit (we have two kits, based either on Stratix II or Stratix IV FPGAs), connected to a daughter board housing the GBT chip. It will allow the test of the 4.8 Gb/s links in each direction. The daughter board can also run in a standalone mode and control the GBT via an I2C interface, to allow full loopback testing. The first wafer of these chips arrived at the end of May 2010. In this paper, we present the GBT prototype chip, his testing features, the system designed to fully qualify the component and the preliminary results obtained.

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