Contribution ID: **106** Type: **Oral**

The Design for Test Architecture in Digital Section of the ATLAS FE-I4 Chip

Wednesday, September 22, 2010 11:50 AM (25 minutes)

This paper describes an original Design-for-Test (DfT) architecture implemented in the ATLAS FE-I4 pixel readout System-on-Chip (Soc) to accommodate the higher quality demands of future generation LHC detectors. To ensure that the highest possible number of fault-free devices is used during the experiment, the so-called production test to detect faulty devices after the manufacturing has to be executed. For that reason, we devised a straightforward and effective DfT circuitry inside the digital part of the FE-I4 that will enable high fault coverage of potential structural faults while maintaining the performance and area penalties of the entire design negligible.

Summary

The next upgrade of ATLAS experiment will make use of a high number of FE-I4 integrated circuits inside the insertable B-layer (IBL). The number of devices necessary for the experiment will be reaching order of magnitude of 100 000, and hence, there is a raising concern on establishing a certain quality level for such a high number. A functional test, no matter how well devised, is not suitable for exhaustive test to ensure that non-faulty devices are used during the experiment. Instead, a focused production testing applying commercial IC testers has to be employed in the FE-I4 product creation process. The production testing makes primarily use of a structural test, which focuses rather on the circuit structure and can cover manufacturing defects that otherwise may not have been detected by functional testing. The examples of those manufacturing defects are e.g. power or ground shorts, open interconnect on the die (caused by dust particles), short circuited source or drain on the transistor, (caused by metal spike through) etc.

The production test effectiveness of complex SoCs depends heavily on the DfT structures implemented inside the chip and needs to be addressed in the early stage of the design. The architecture that we devised is based on "Divide and Conquer" approach with full scan through the sequential elements of the circuits. FE-I4 has a modular structure and the DfT architecture contains one scan chain for each of the digital modules with random logic. The DfT structures contain the so-called wrappers built around each port of the modules to enable complete isolation among each of the modules in the design as well as between the functional and test modes within the module. This is particularly useful in the multi-site project where each of the designers is free to focus on his module without worrying on the side-effects of a test strategy within another module. The DfT structures are tackled during the conceptual phase and synthesized together with functional portion of the module, i.e. the DfT strategy has been fully integrated into the design flow. A Synopsys TetraMax automatic test pattern generator tool has been employed to calculate the test patterns and the fault coverage based on the test structures and test setting modes. Moreover, the tool also carried out the translation of the test patterns into the real test vectors with timing information running on a commercial IC tester. Preliminary results with regard to the test using this approach are encouraging. The level of fault coverage for certain modules reaches the figures above 90%. In addition, thanks to the seamless design and test flow, performance degradation and area overhead are negligible at an absolute scale.

Primary author: Dr ZIVKOVIC, Vladimir (NIKHEF Institute)

Co-author: Dr GARCIA-SCIVERES, Maurice (Lawrence Berkeley National Lab., Berkeley, CA, USA)

Presenter: Dr ZIVKOVIC, Vladimir (NIKHEF Institute)

Session Classification: ASICs

Track Classification: ASICs