A pixel read-out architecture implementing a two-stage token-ring, zero-suppression and compression

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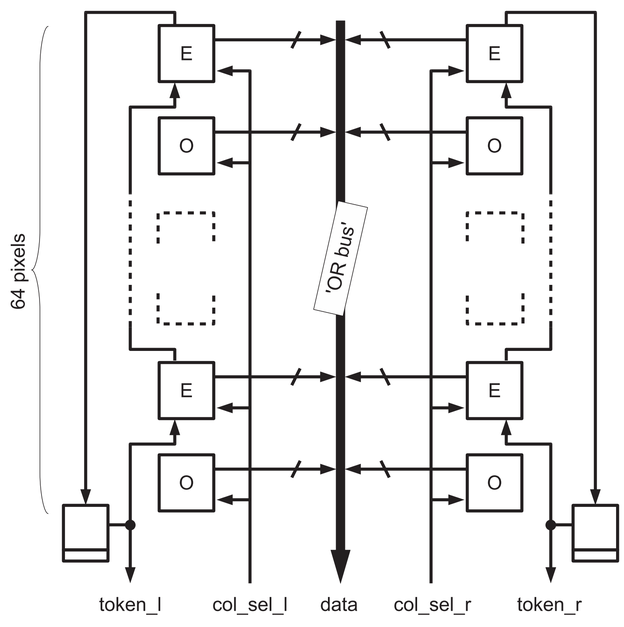
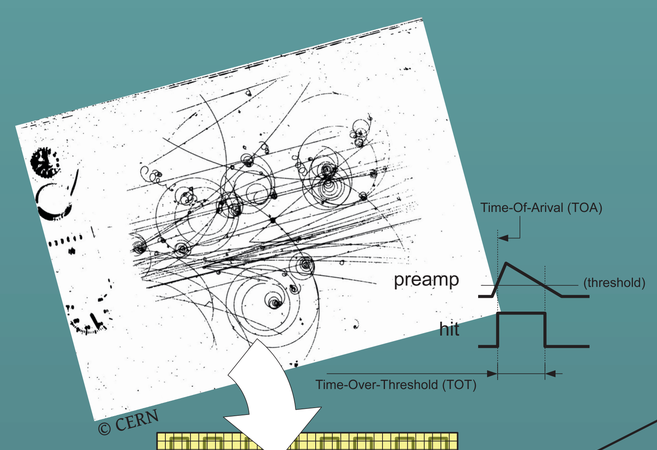
A C++ model of a read-out architecture for the new LHCb pixel detectors has been developed. The read-out is inherently zero-suppressing due to the use of multiple token-ring layers. Data compression is achieved by creating pixel pairs inside the pixel array. The system can be adapted to different illumination gradients to reduce hit data loss. The architecture has been simulated for functionality and loss-performance.

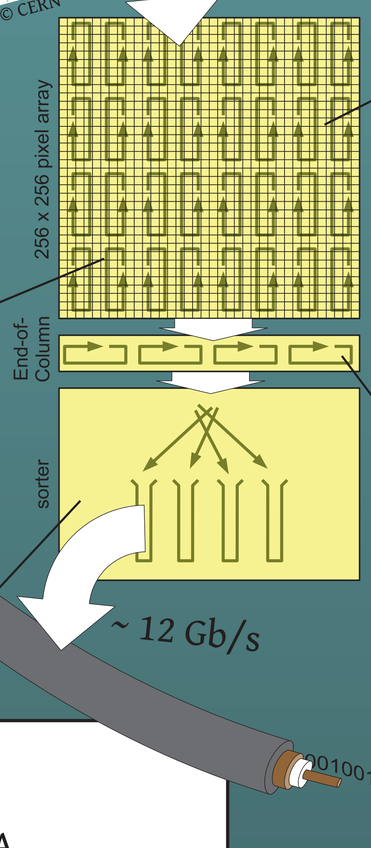
Simulation of the 'hottest' chip:
- 40 MHz Bunch-Crossing ID clock (BCID)
- re-sampled data from event generator
- average Time-Over-Threshold: ~ 8 BCID
- average illumination: ~ 290 Mhits/cm^2/s
- peak illumination: ~ 930 Mhits/cm^2/s

Column-pairs and column token-rings

- zero-suppression
- bus arbitration
- hardware sharing
- column-pairs form 256 x 256 pixel array (4 rows x 128 columns of column-pairs)







- 55 um x 55 um pixels
- 1.4 cm x 1.5 cm chip size
- pixel array: ~ 6.3 Mgates; ~ 250 mW (including data bus power)
- EoC and sorter: ~ 350 kgates; ~ 90 mW

Pixel pairs

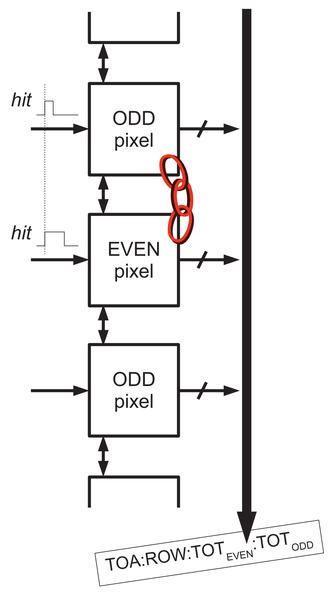
- only even pixels can hold TOA
- odd pixels find a neigbouring even pixel to combine with

- share TOA
- share row address
- share hardware

- 45% of packets contain two hits

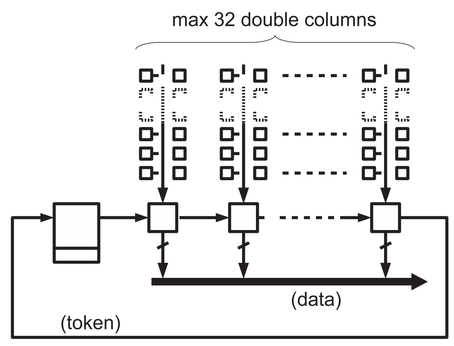
compressed to:

~ 79%



End-of-Column token-rings

- 32 variable-length EoC token-rings
- zero-suppression
- adaptable to illumination gradient
- low hit loss[1] at the pixel level



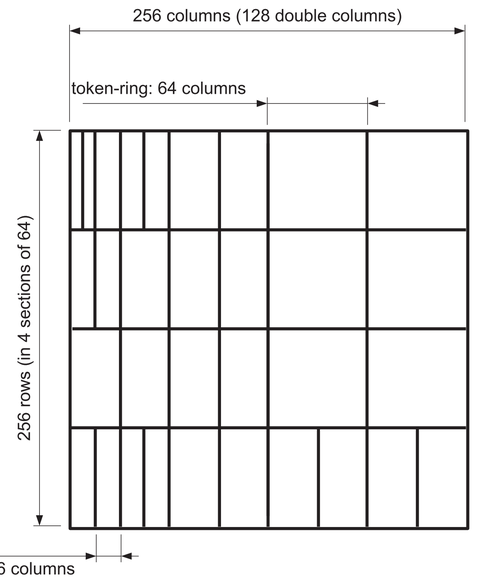
pixel-level hit loss[1]:

< 1%

+ beam

array-level hit loss[1]:

~ 0.3%



Sort and output

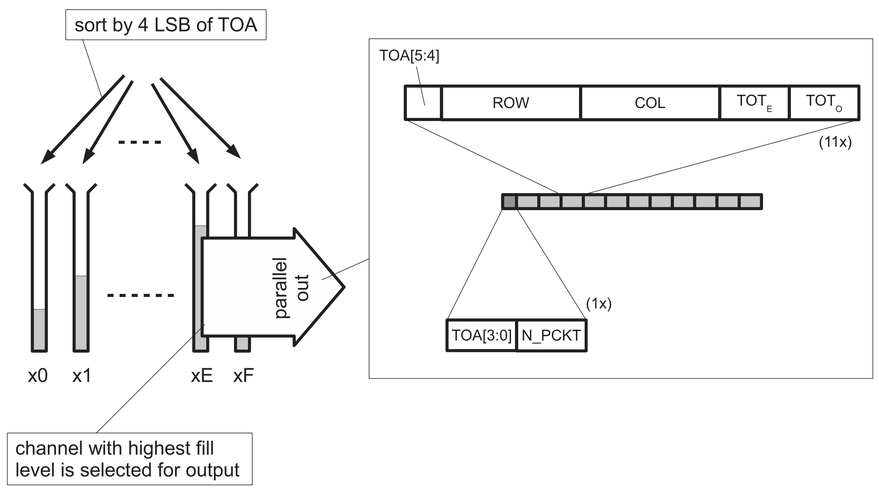
- further compression by grouping by TOA

total compressed to:

~ 70%

sorter FIFO loss:

~ 0.3%



[1]) hit loss: an occupied/unread pixel is hit and new data cannot be recorded.

Summary

Reduction of hit loss: less than 1% hit loss
- Token-ring based read-out; short waiting times.
- Adaptable End-of-Column token rings for optimum read-out speed depending on illumination.

Data compression: data rate of the 'hottest' chip reduced from 17 Gb/s to 12 Gb/s
- Zero-suppression by use of token-rings.
- Creation of pixel pairs.
- Removal of part of redundancy in Time-of-Arrival values.

Implementation
- VHDL implementation of the pixel logic in the limited available space below each pixel was succesful.

Plans:
- Simulation of timing of the column data buses (long lines across columns) and token-rings.
- Investigation into effects of and fixes for single-event upsets and stuck pixels.