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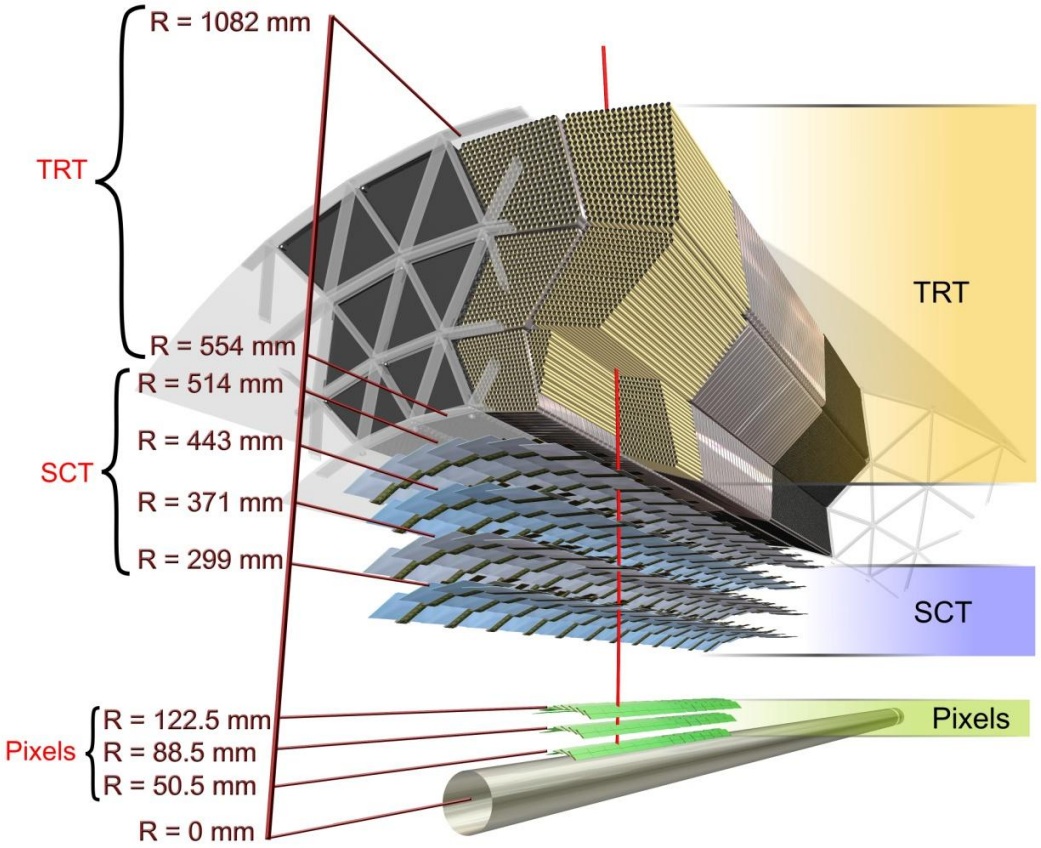
The FE-I4 Pixel Readout System-on-Chip for ATLAS Experiment Upgrades

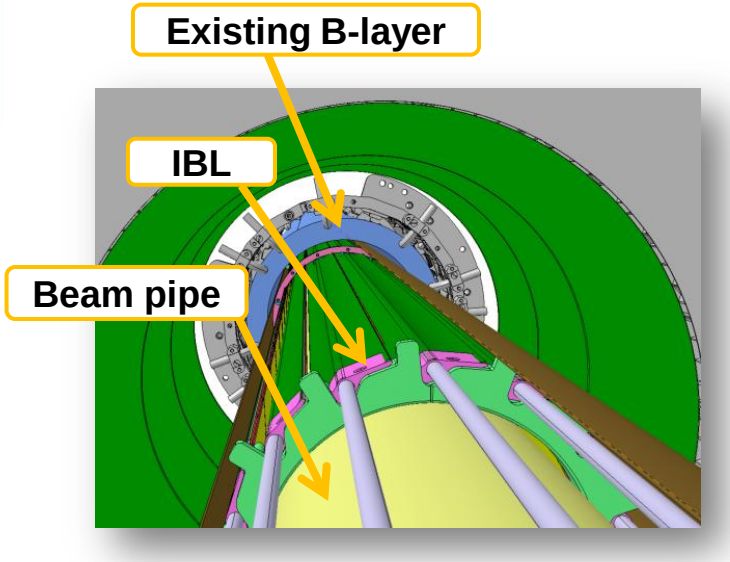
Tomasz Hemperek on behalf of ATLAS Pixel Collaboration

ATLAS Detector



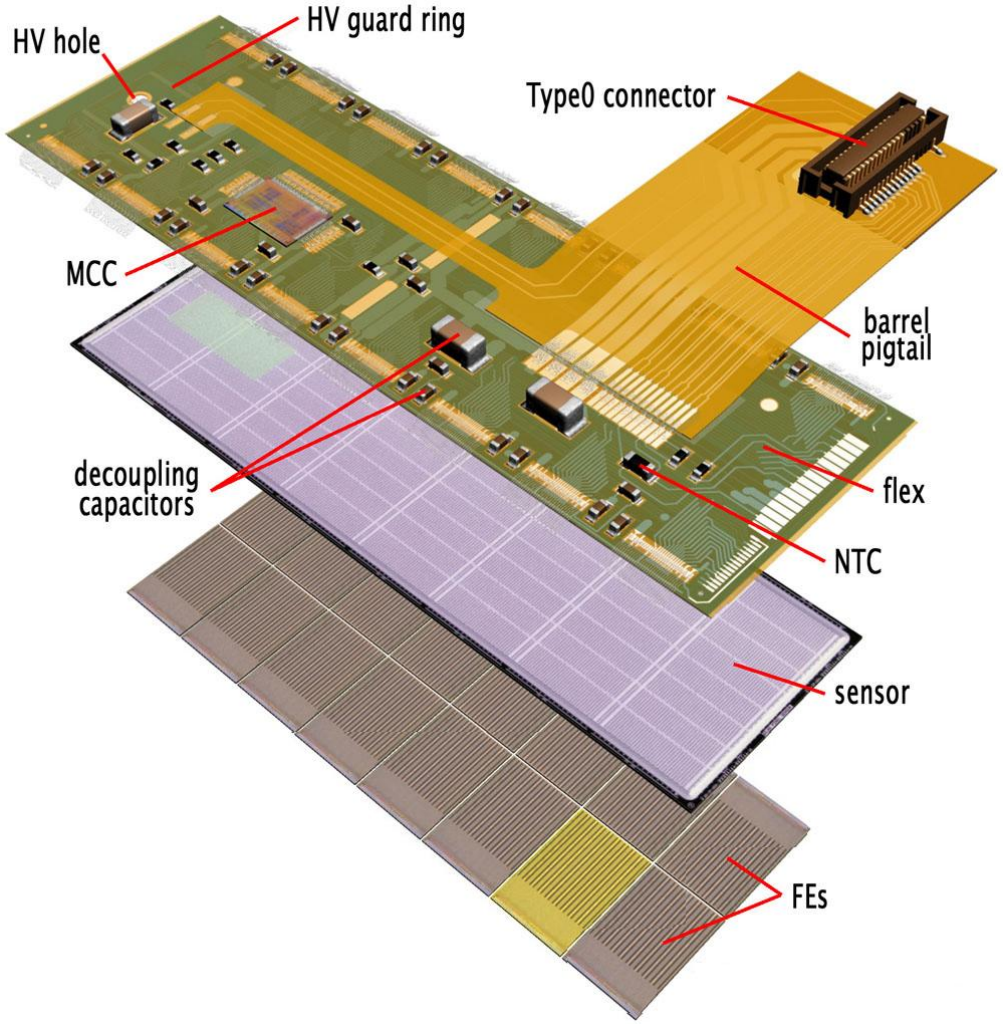
Pixel Detector:

- 3 barrels
- 112 staves
- 1744 modules
- 80 million channels



IBL = New Insertable B-Layer at 33 mm

Current Pixel Detector Module



- 16-front-end chip (FE-I3) module with a module controller chip (MCC)
- Planar n-on-n DOFZ silicon sensors, 250 µm thick
- Designed for for 1 x 10^{15} 1MeV n_{eq} fluence and 50 MRad

Front End Chip

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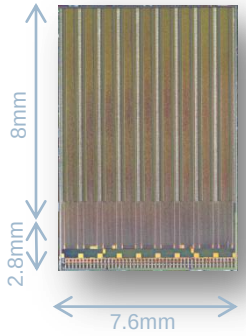
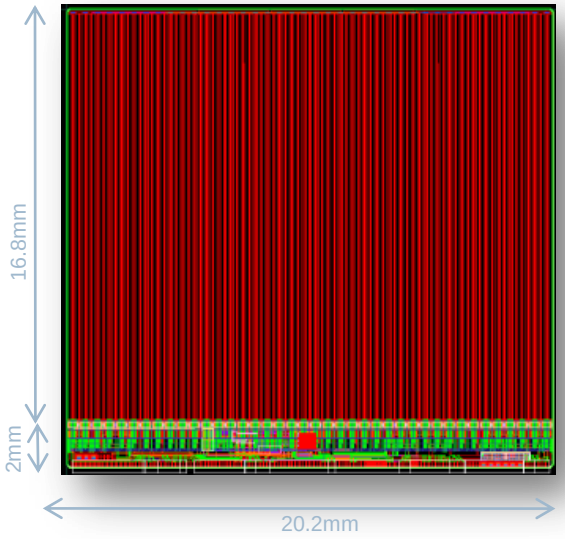
FE-I3



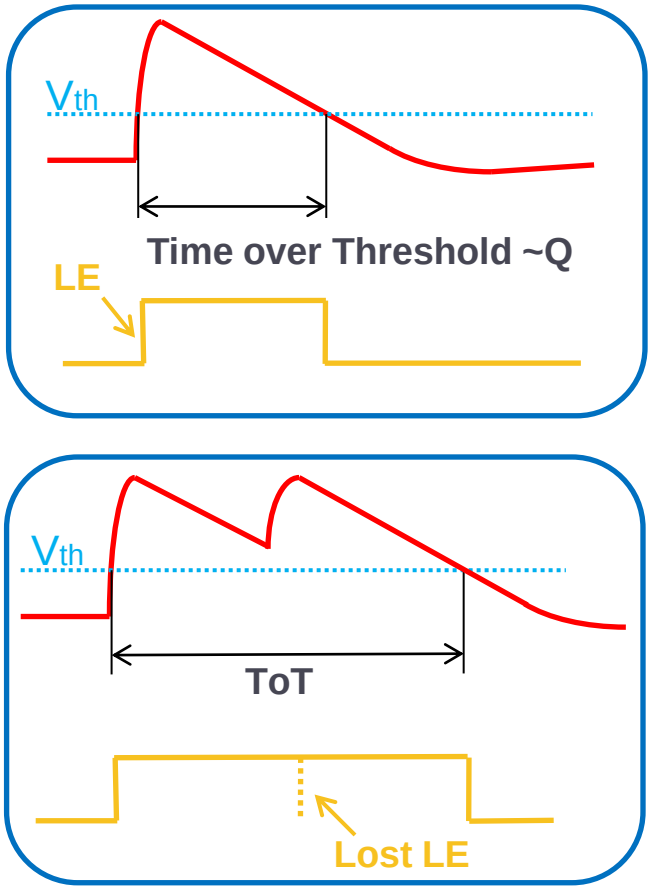
FE-I4



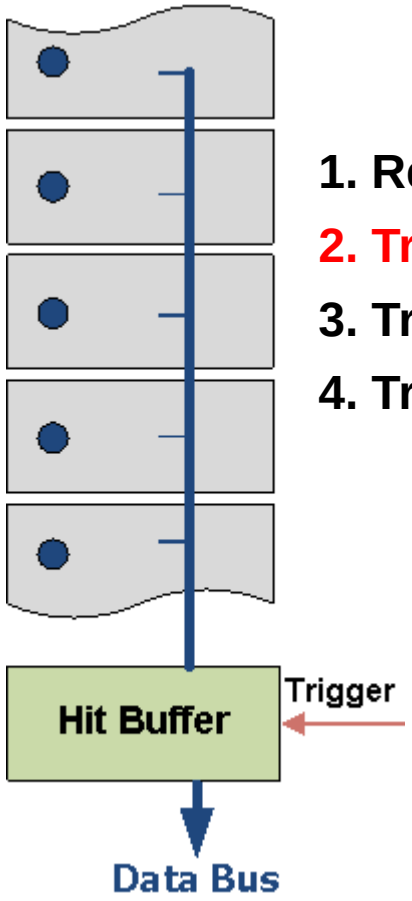
Pixel Size [µm²]	50×400	50×250
Pixel Array	18×160	80×336
Chip Size [mm²]	7.6×10.8	20.2×19.0
Active Fraction	74 %	89 %
Output Data Rate [Mb/s]	40	160
Transistor Count [M]	-	~80

Inefficiencies

Double Hit

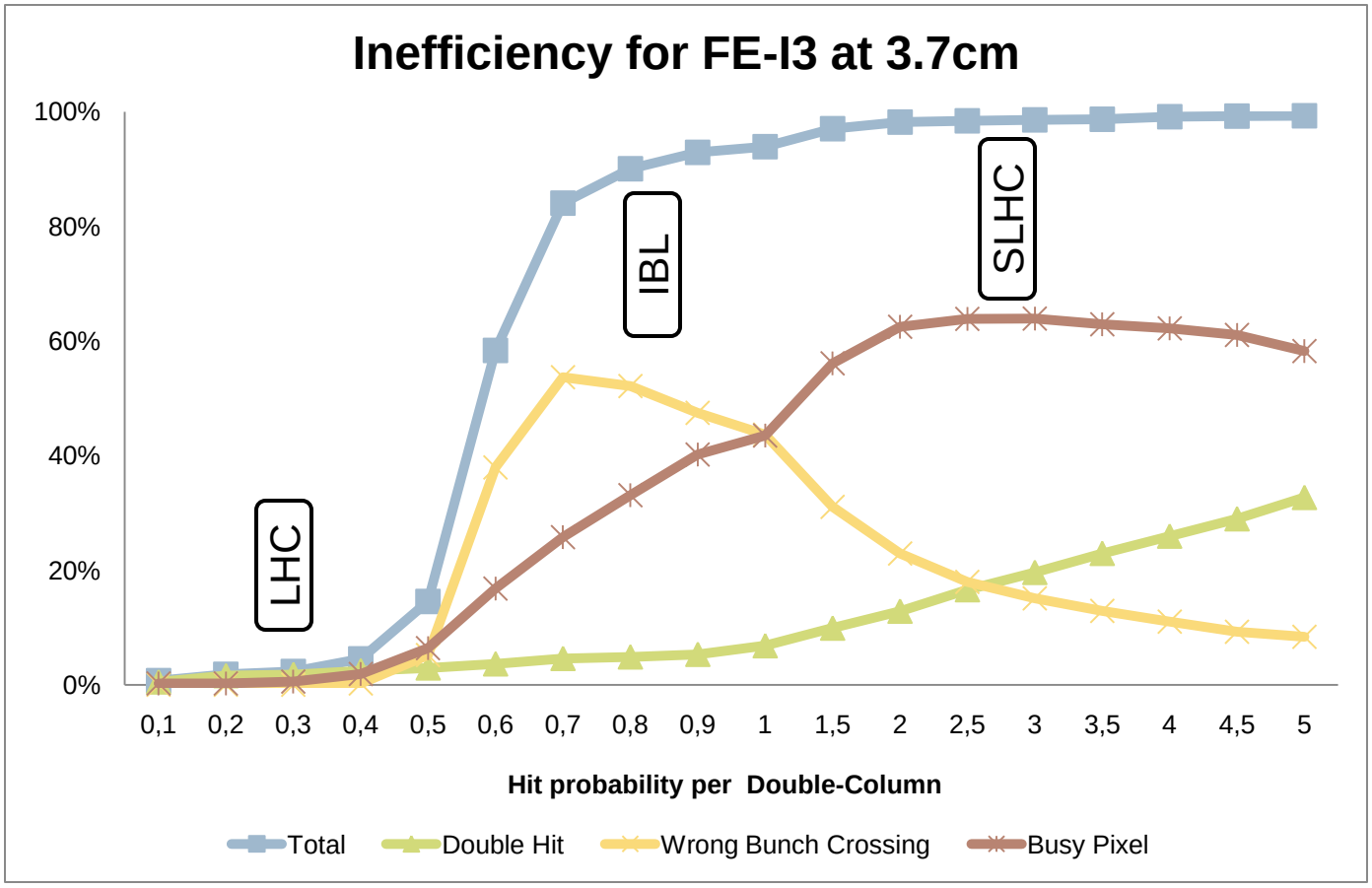


Column Waiting (FE-I3)



1. Record
2. Transfer
3. Trigger
4. Transmit

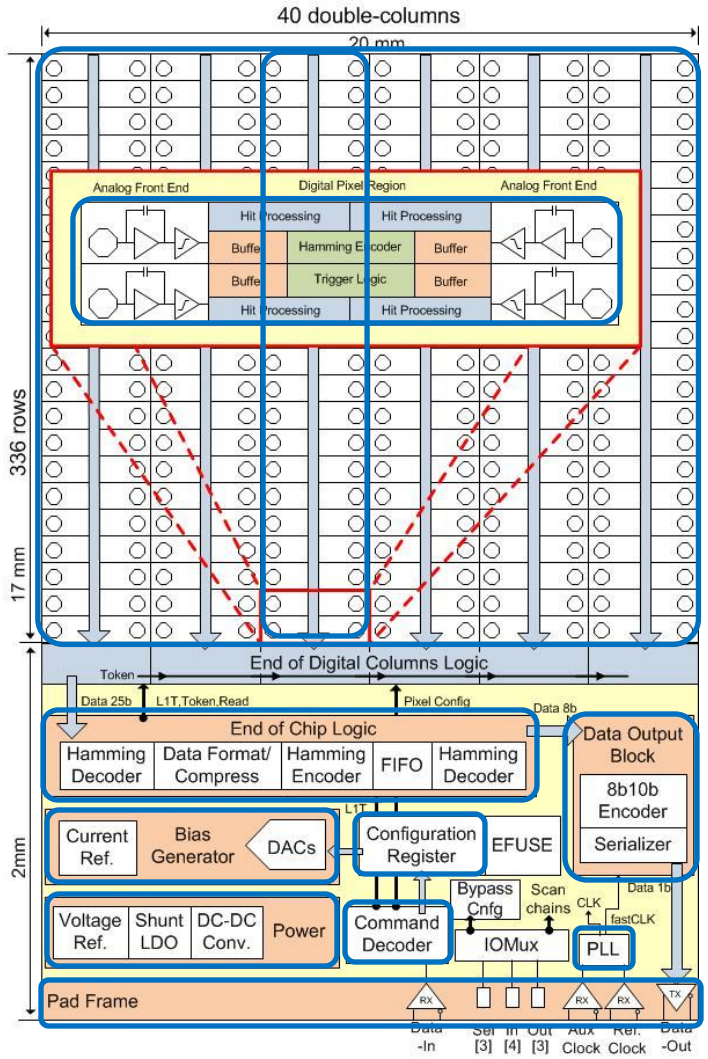
Motivation


Inefficiency for FE-I3 at 3.7cm
100%
80%
60%
40%
20%
0%
LHC
IBL
SLHC
0,1
0,2
0,3
0,4
0,5
0,6
0,7
0,8
0,9
1
1,5
2
2,5
3
3,5
4
4,5
5
Hit probability per Double-Column
Total
Double Hit
Wrong Bunch Crossing
Busy Pixel

New FE improvements

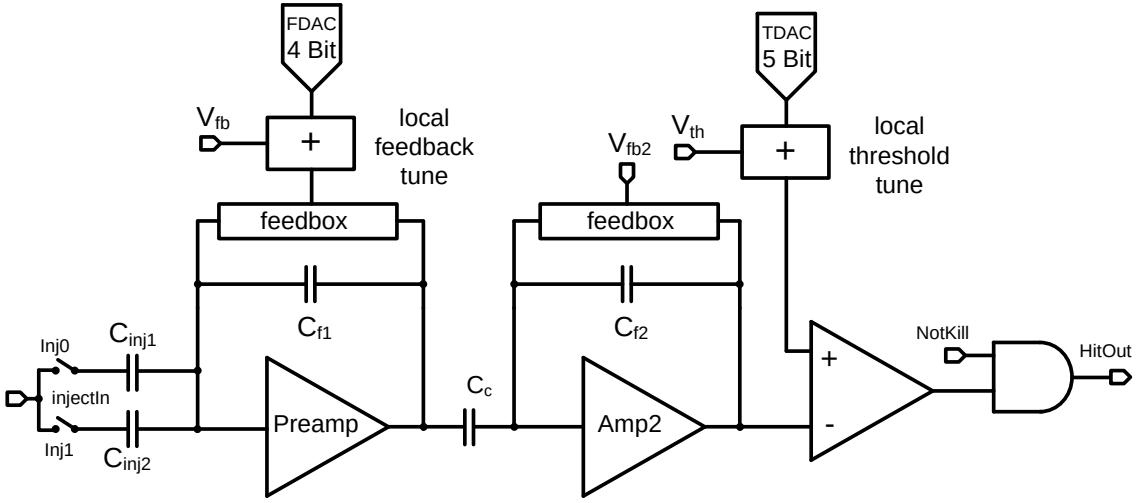
- New technology
- Smaller pixel size
- Bigger chip size and active area
- New digital architecture
- New analog pixel
- Reduce number of external components
- New powering schemes
- Decrease cost (per area)
- Better radiation hardness

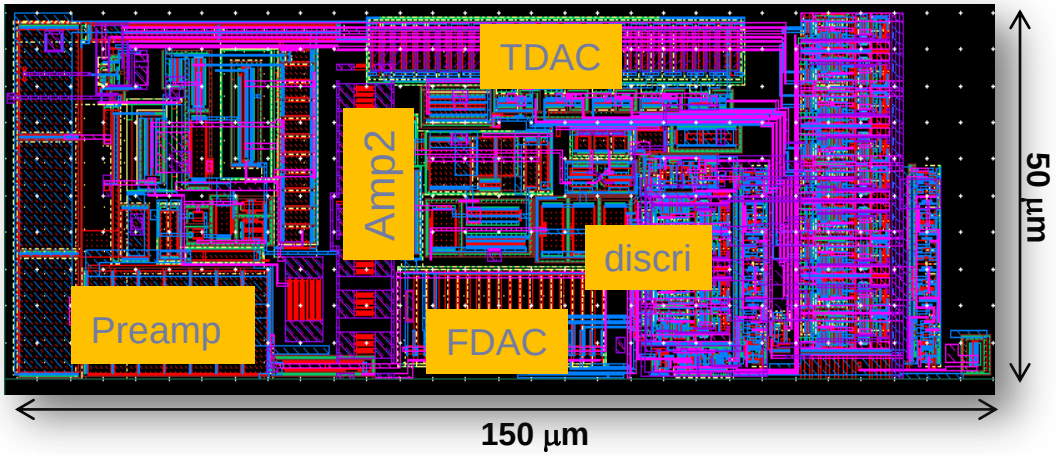
FE-I4 Functional Overview



- Pixel Array
- Double Column
- 4 Pixel Region
- End Of Chip Logic
- Data Output Block
- Phase Lock Loop
- Command Decoder
- SEU-Hard Memory
- DACs & Reference
- Power
- Pads / RX /TX

Analog Pixel

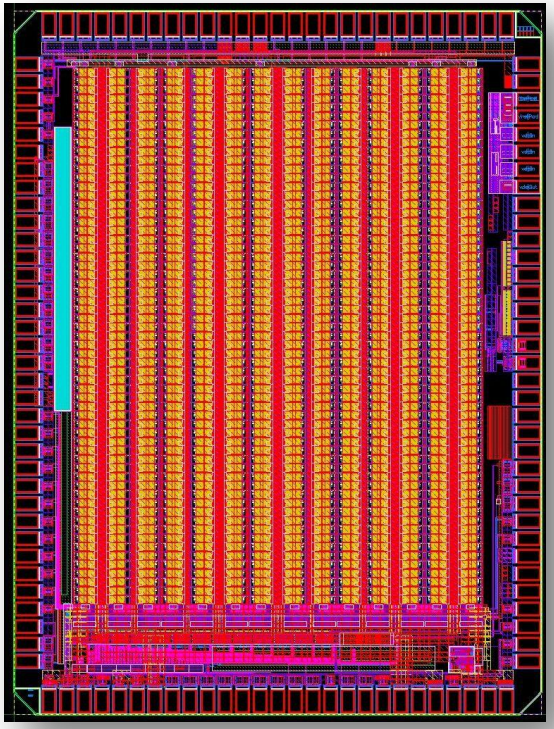




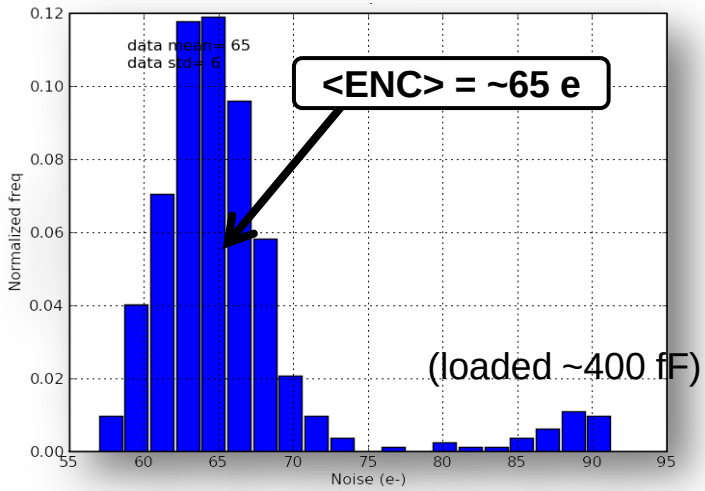
- Two-stage architecture optimized for low power, low noise and fast rise time
- Additional gain Cc/Cf2~ 6
- More flexibility on choice of Cf1
- Charge collection less dependent on detector capacitor
- Decoupled from preamplifier DC potential shift caused by leakage
- Local DACs for tuning feedback current and global threshold
- Charge injection circuitry

FE-I4-P1 (Prototype)

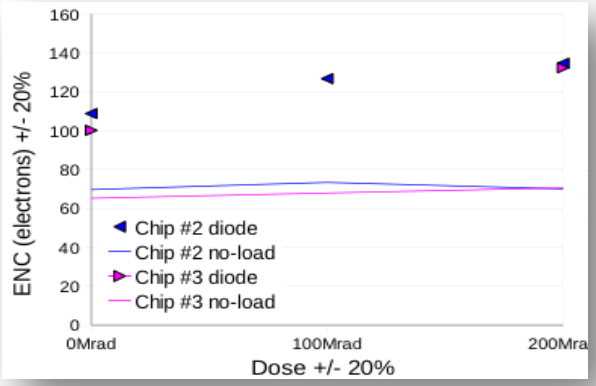
- 61x14 pixel array
- Silicon proven
- RadHARD up to 200MRad



Noise Measurements

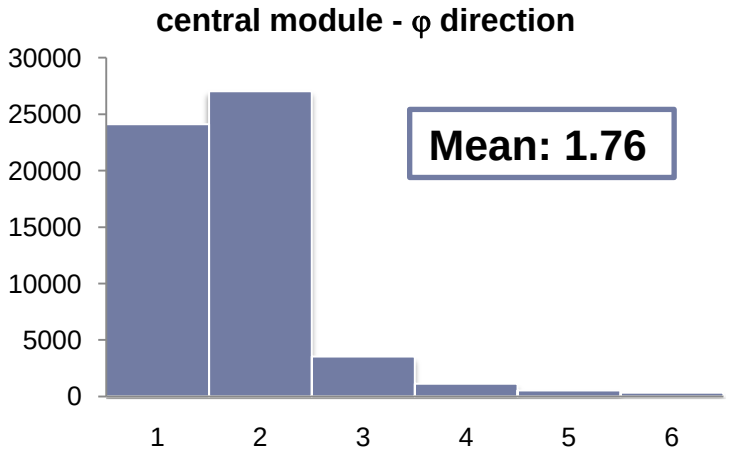


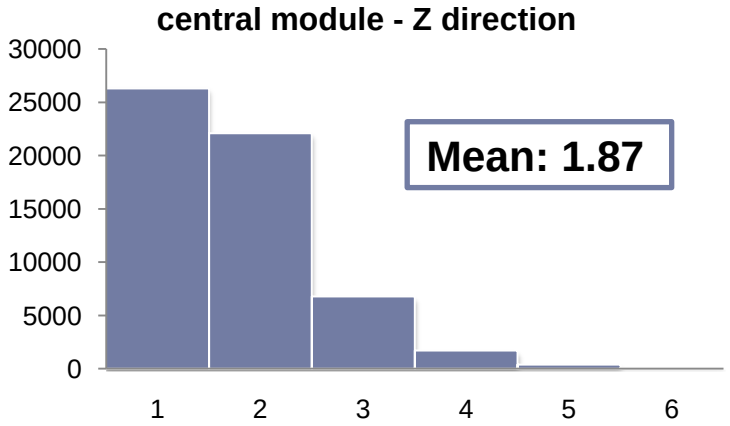
Noise Measurements (Irradiation)



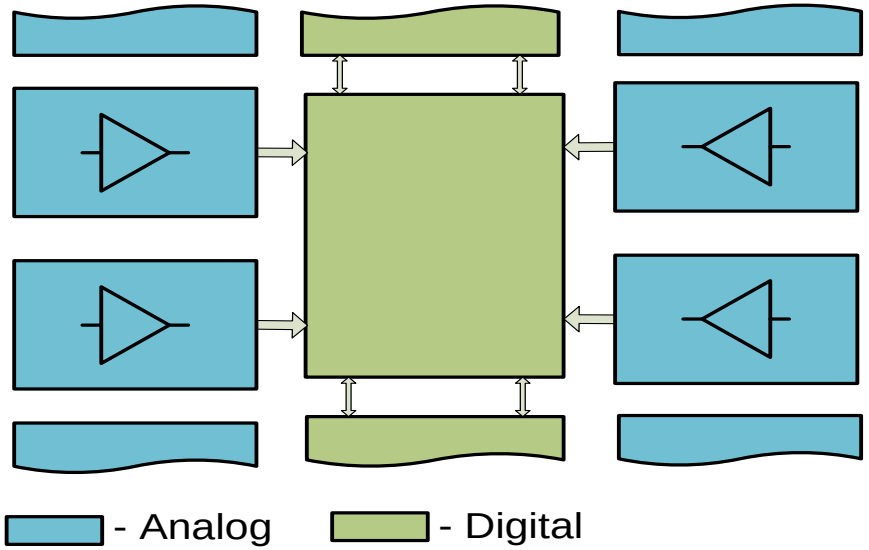
4 Pixel Region

Cluster size projection



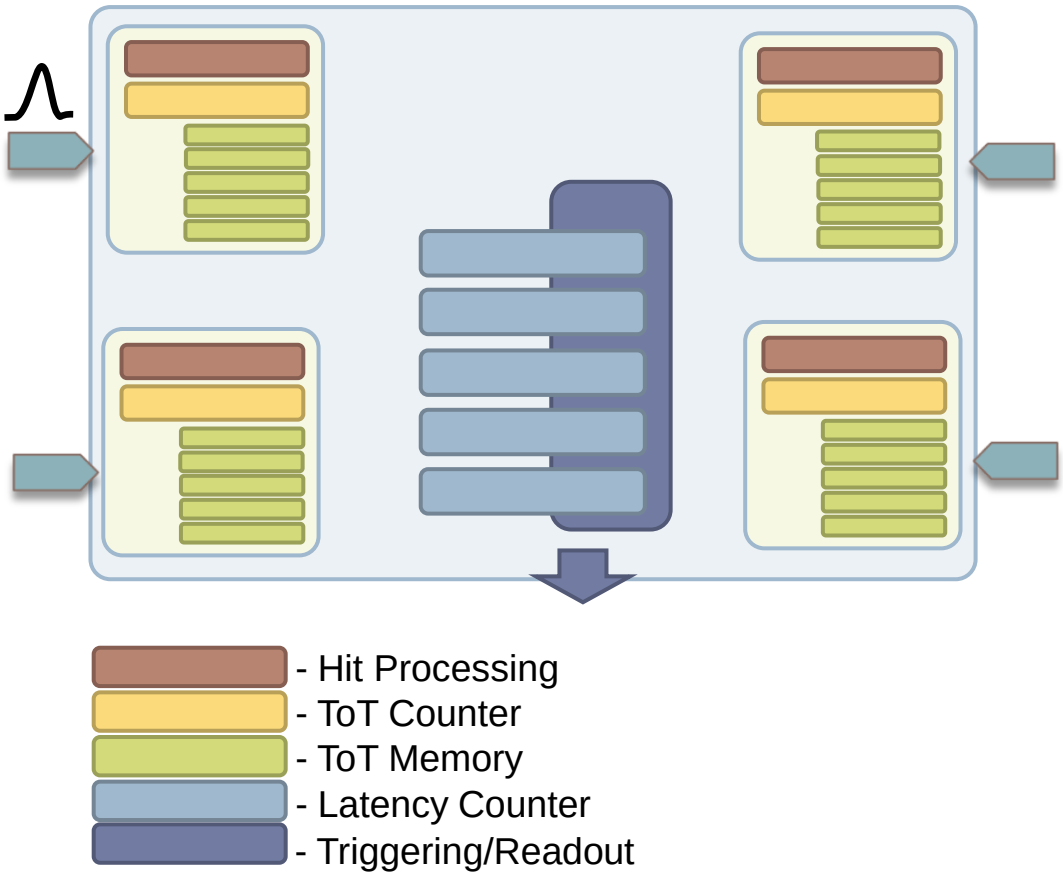


Pixel organization



- 4 analog pixels are connected to one digital region
- Analog pixels can operate and be tested independently from digital part

Digital Region (simplified)



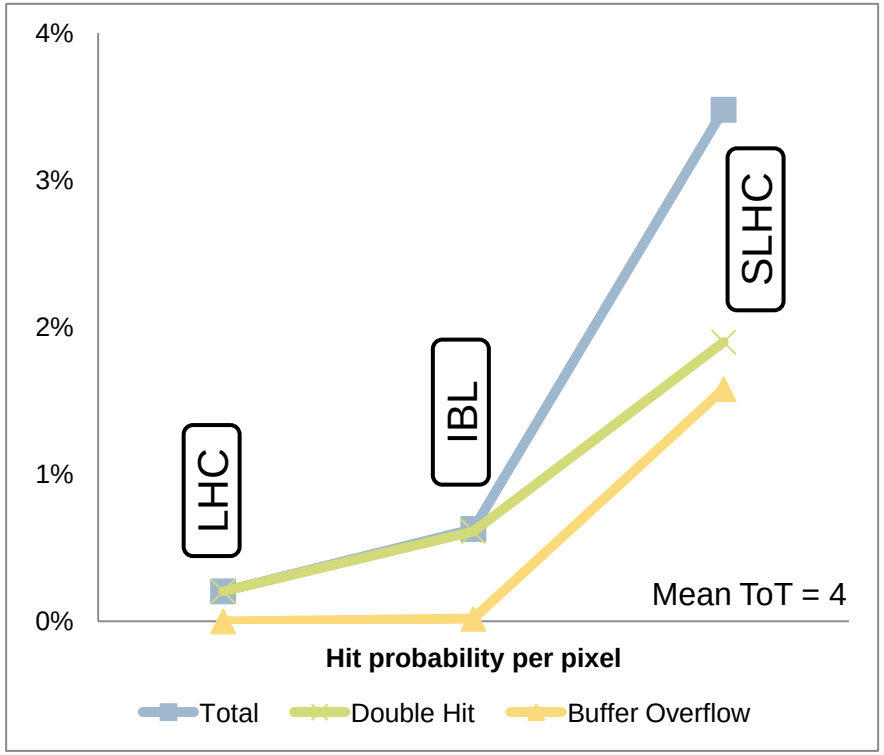
- Receiving hit
- Generate leading edge
- Start ToT counter
- Assign first free memory and latency counter
- Generate trailing edge
- Store ToT value
- Check for trigger when latency counter finished
- Indicate ready to read status (release token)
- Read memory
- Release memory after read

FE-I4 Inefficiency

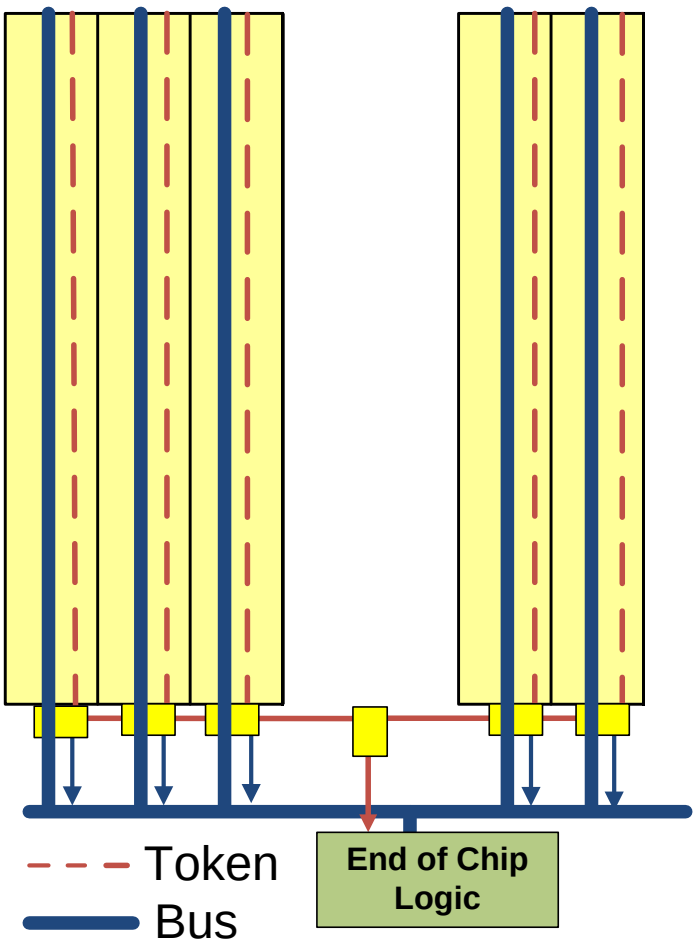
Regional Buffer Overflow

Memories	Simulation	
	IBL	10xLHC
5	0.047%	2.19%
6	0.011%	0.65%
7	<0.01%	0.16%

FE-I4 Inefficiency (3.7cm)

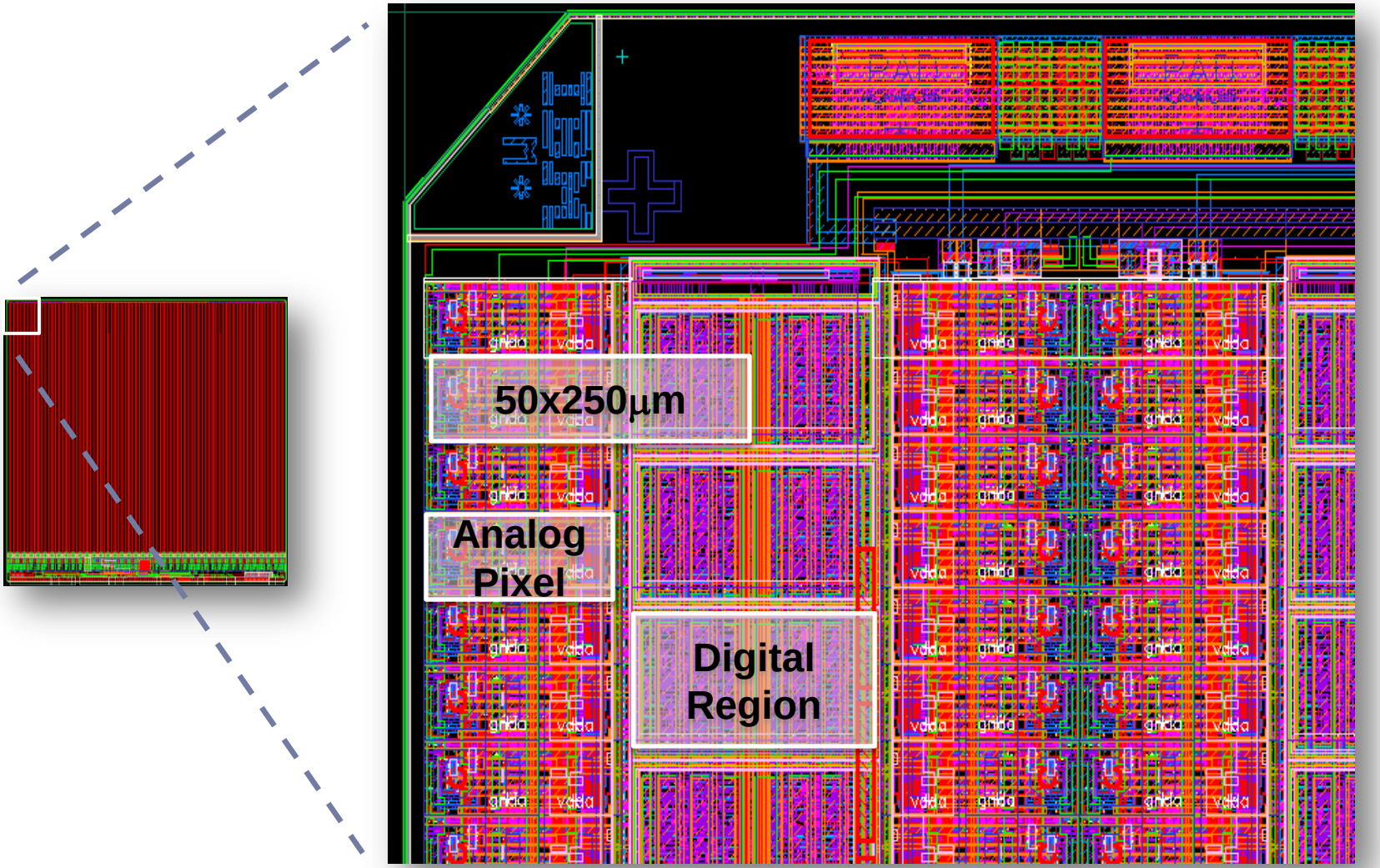


Column Readout

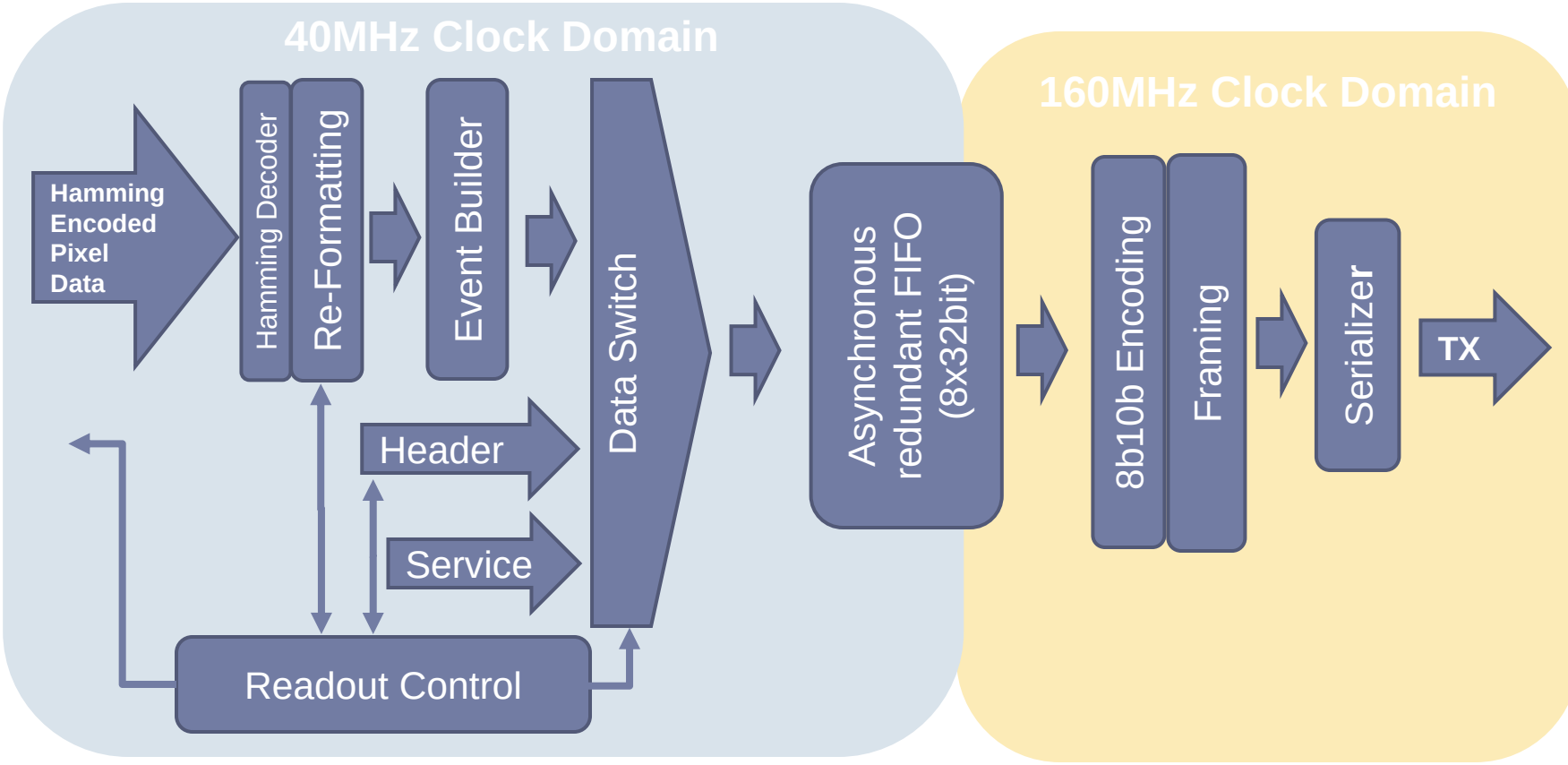


- Two prioritized token scenario (column and periphery level)
- One data bus
- End of column logic selects column to read
- Chip control logic controls trigger and read
- Data is always read in the same order
- All buses including address (thermal encoded) protected with hamming encoding

Pixel Array Layout



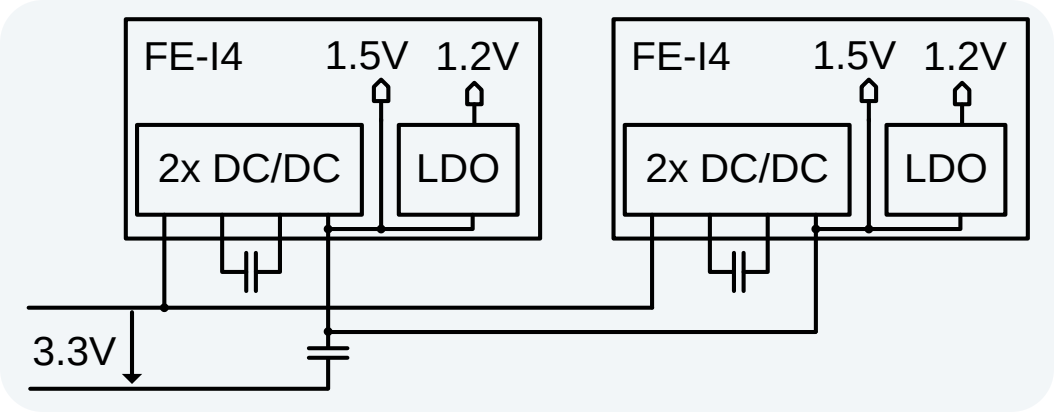
Framing / Transmission



Re-formatting: Data reduction about 25% and 8-bit word format

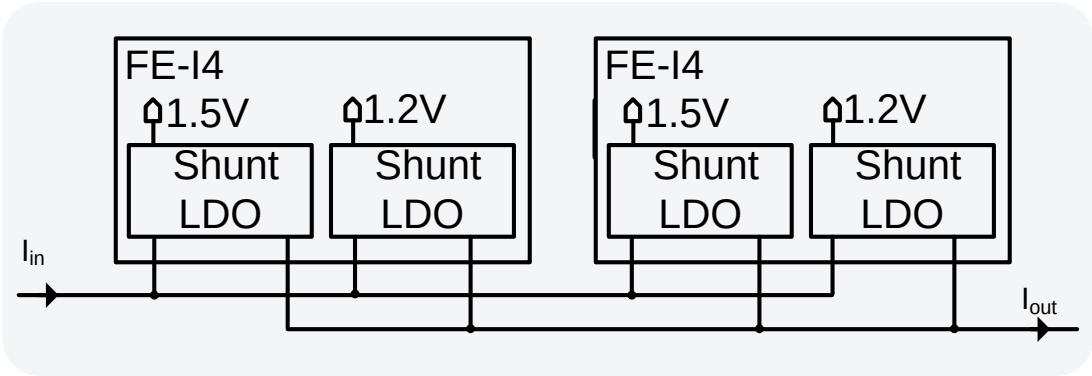
Powering

DC/DC



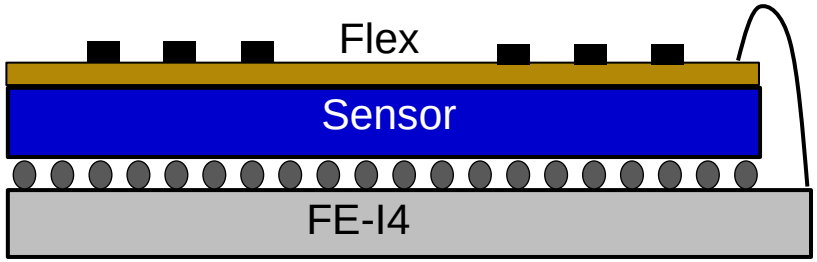
- Saving cable material budget
- Reduction of cable power losses

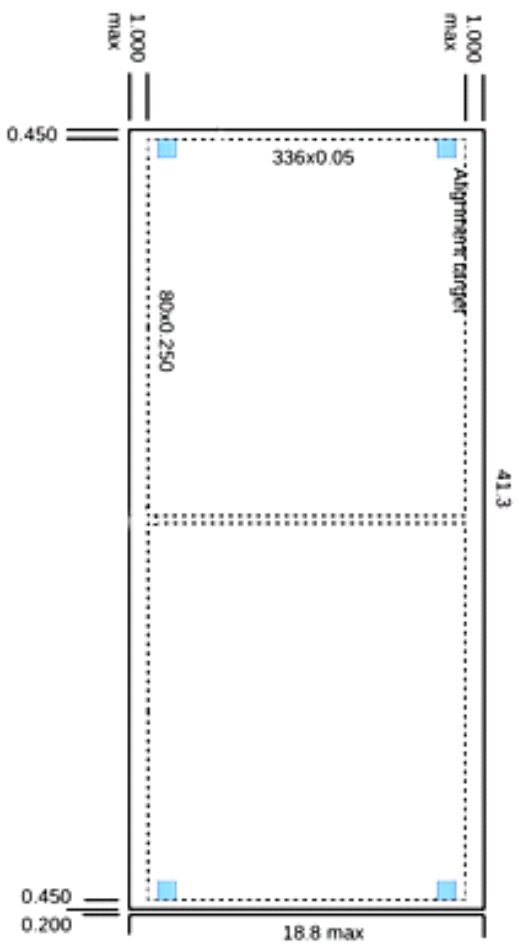
Serial Power



New Module Concept

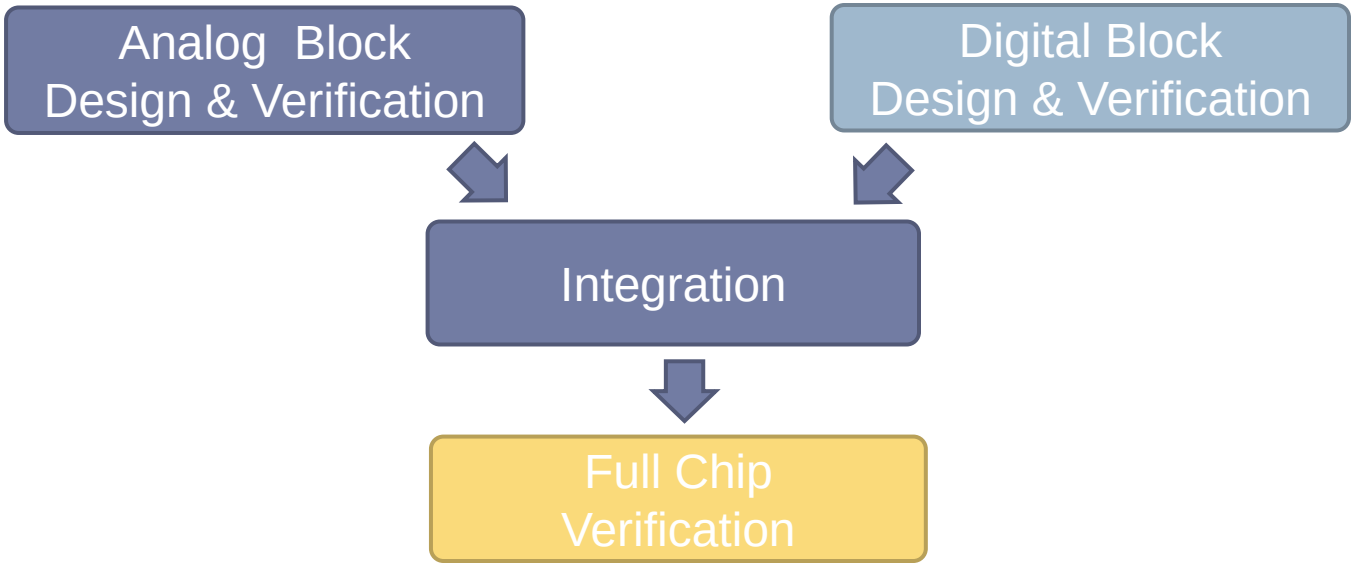
- Sensor technology independent.
- Decision on sensors after prototyping with FE-I4
- Minimum amount of external components





Design Flow

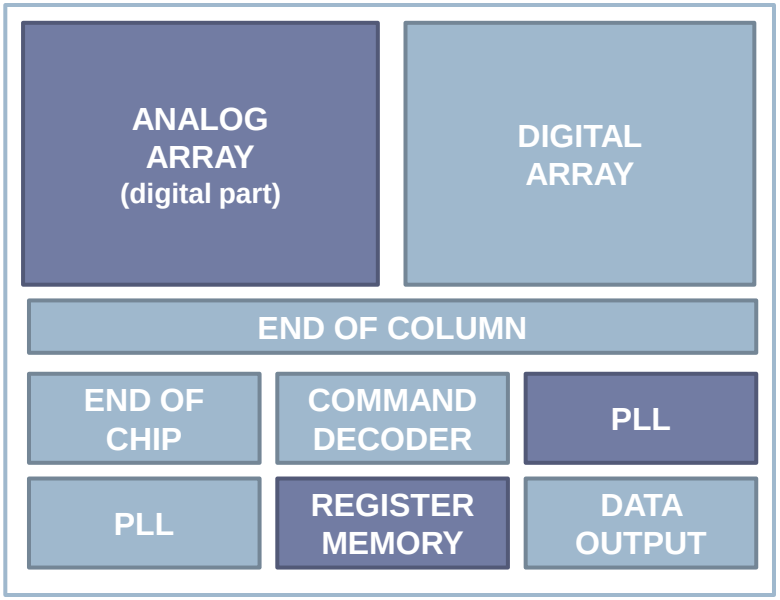
- Design in “big A small D” methodology
- Blocks designed and verified individually
- Full chip digital and mixed-signal verification
- Work synchronization with integrated Revision Control System
- Big chip = many difficulties with software and PDK!



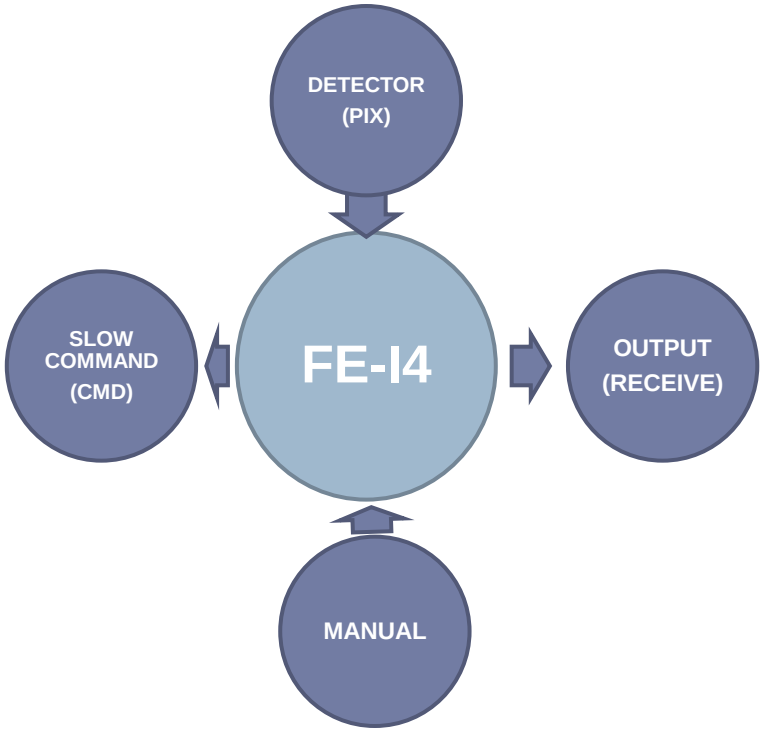
Verification

- Full chip verification based on Open Verification Methodology (OVM) with multiple physics based and random test

Modeling



Interfaces



Conclusion

- Project duration: ~3 years
- Design team: ~21 persons+

- FE-I4A last official shipping date: This Thursday (23rd September 2010)
- Test setup readiness ramping-up, on time for IC back
- Tests: Wafer, single-chip, bump-bonded (planar, 3D, diamond), irradiation

Design team

Bonn: D. Arutinov, M. Barbero, T. Hemperek, A. Kruth, M. Karagounis
CPPM: D. Fougeron, F. Gensolen, M. Menouni
Genova: R. Beccherle, G. Darbo
LBNL: S. Dube, D. Elledge, J. Fleury (LAL), M. Garcia-Sciveres, D. Gnani, F. Jensen, A. Mekkaoui
NIKHEF: V. Gromov, R. Kluit, J.D. Schipper, V. Zivkovic

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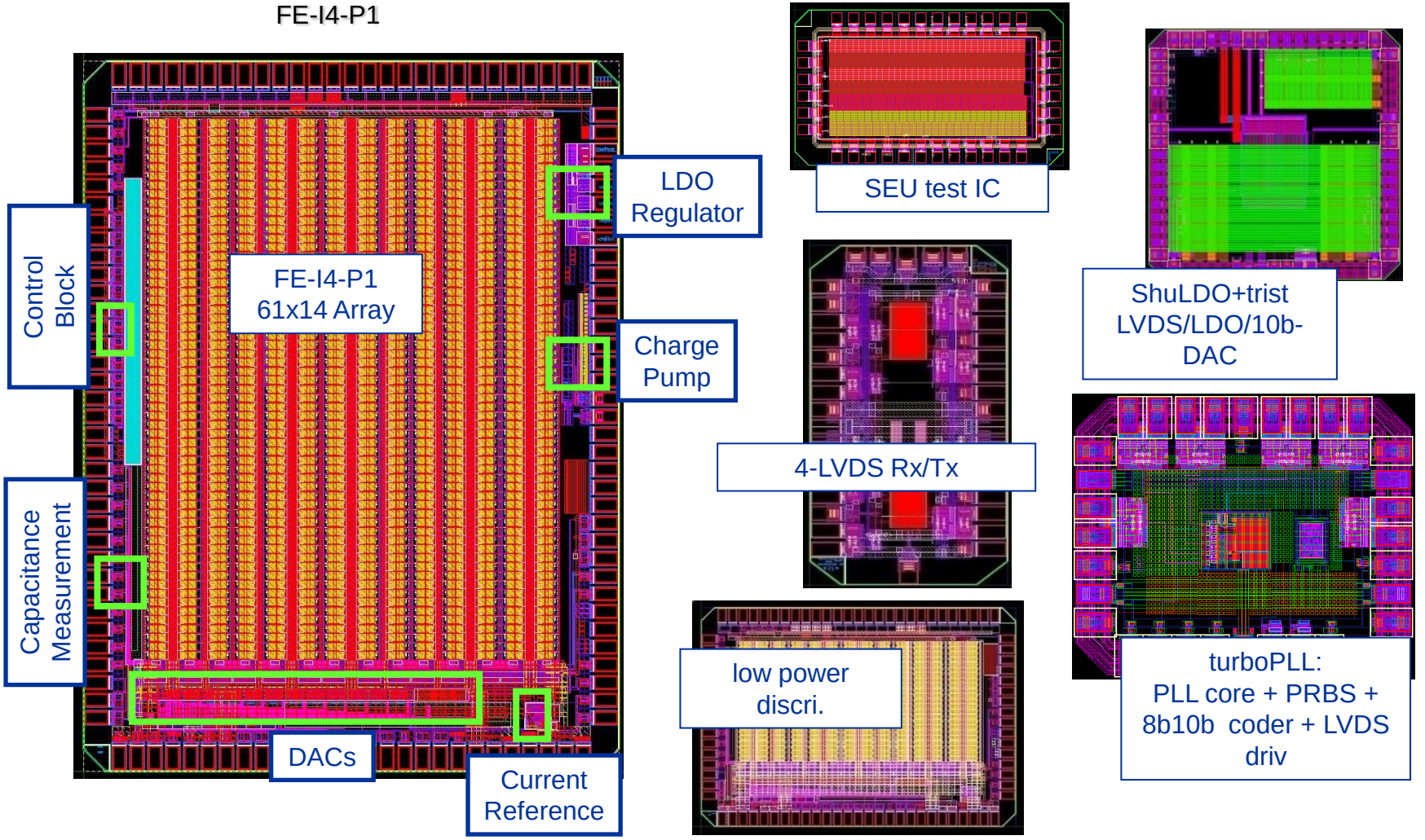
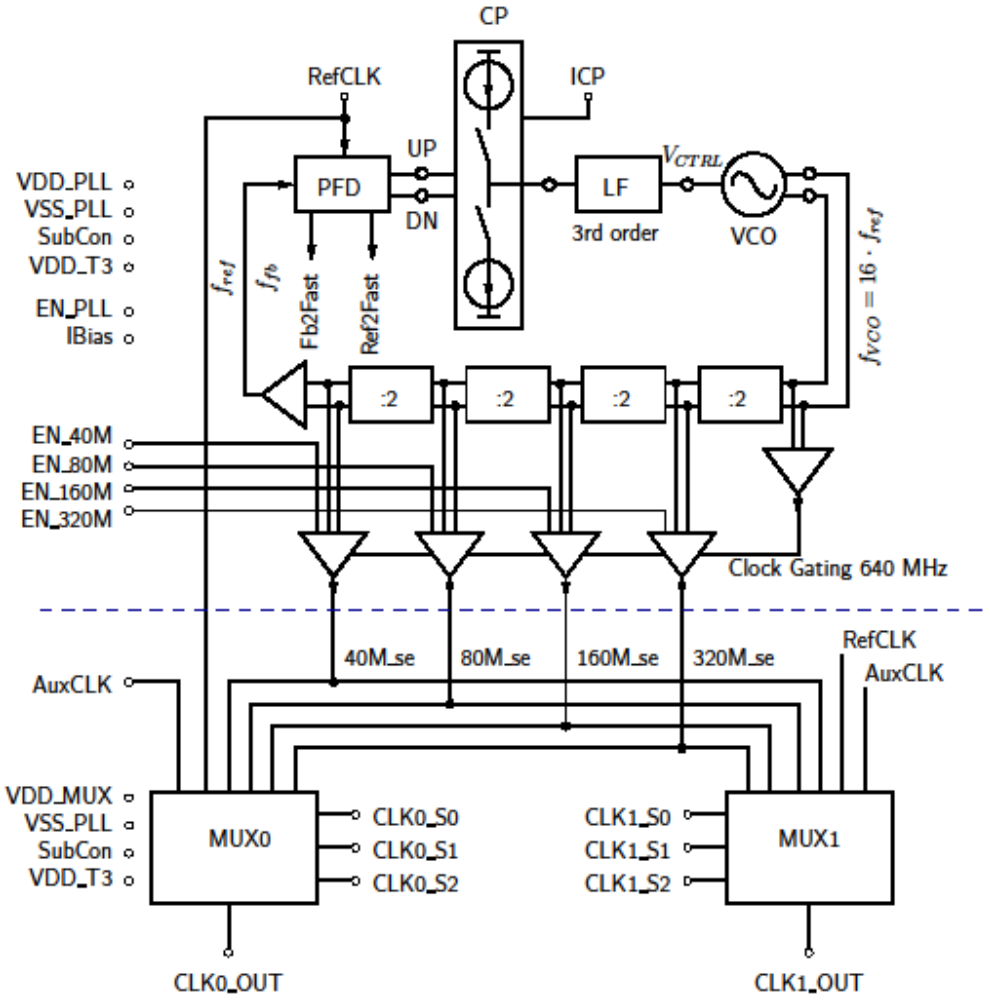
Extra Slides

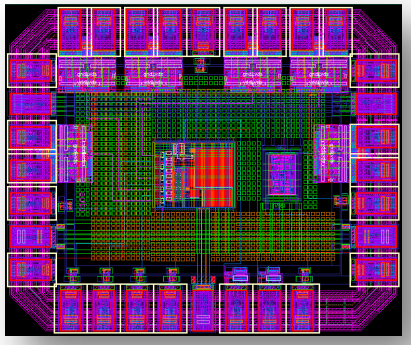
Test Chips


FE-I4-P1
Control Block
FE-I4-P1 61x14 Array
LDO Regulator
Charge Pump
Capacitance Measurement
DACs
Current Reference
SEU test IC
ShuLDO+trist LVDS/LDO/10b-DAC
4-LVDS Rx/Tx
low power discri.
turboPLL: PLL core + PRBS + 8b10b coder + LVDS driv

Clocking

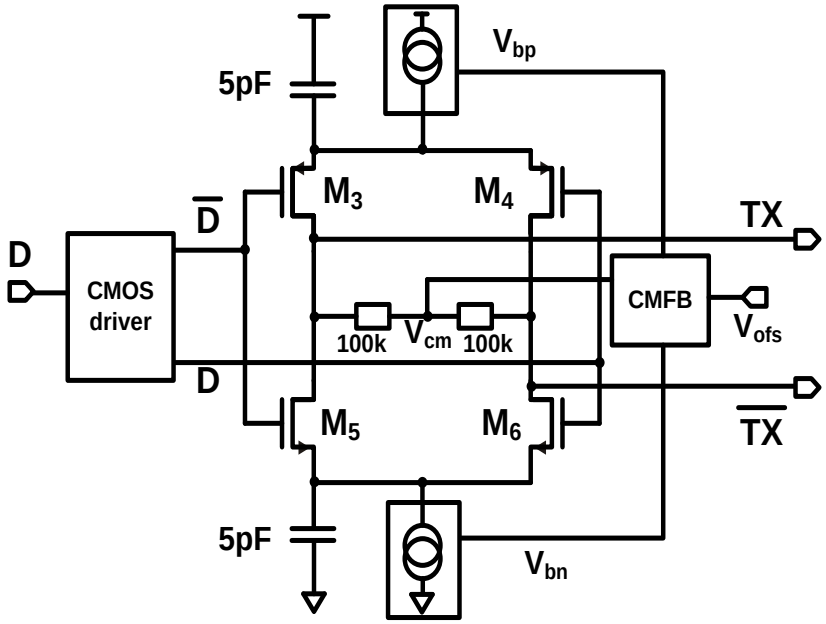


- Phase Lock Loop (PLL) type 2
- Voltage Controlled Oscillator (VCO) at 640 MHz (x16)
- Lost of Lock Detection
- 2 Independent output multiplexers
- Silicon Proven

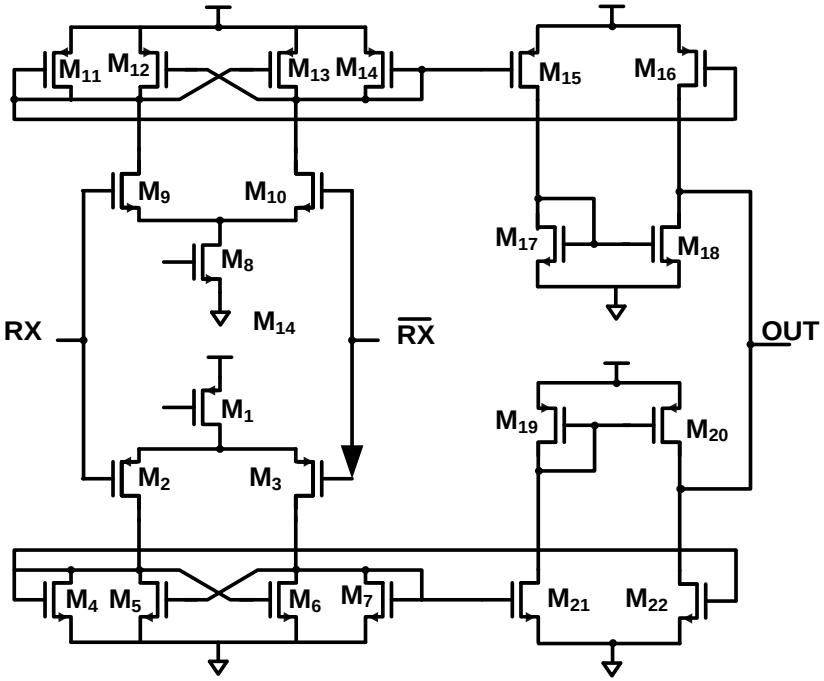


Data Transmission

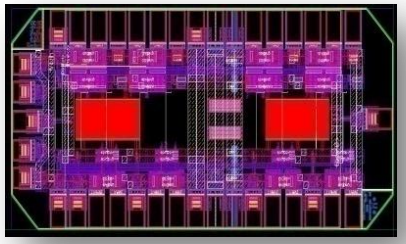
LVDS TX



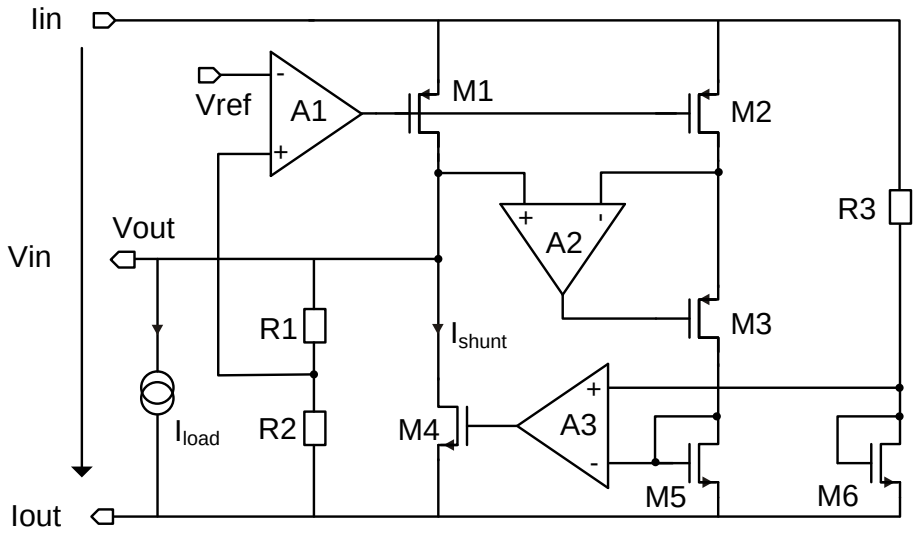
LVDS RX

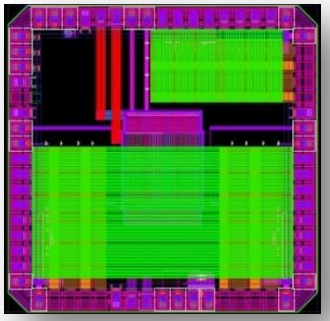


- Transition speed up to 330 MHz
- RadHARD up to 200MRad
- Silicon Proven



Shunt-LDO





- Combination of LDO and shunt transistor
- „Shunt-LDO“ regulators having completely different output voltages can be placed in parallel without any problem regarding mismatch & shunt current distribution
- „Shunt-LDO“ can cope with an increased supply current if one FE-I4 does not contribute to shunt current e.g. disconnected wirebond
- Can be used as an ordinary LDO when shunt is disabled
- Silicon Proven

RadHARD Memory

- Silicon Proven
- RadHARD and SEU Tolerant