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The FE-I4 Pixel Readout System-on-Chip for ATLAS Experiment Upgrades

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This article elaborates on a novel pixel readout system-on-chip (SoC) that has been designed to meet the ever increasing demands of the present and future generation of LHC pixel detectors. The FE-I4 architecture has higher luminosity and rate capability as well as a smaller single pixel area compared to its predecessors and is currently the most complex chip designed for particle physics applications. The IC has been designed in 130nm CMOS technology. The state of the art of the FE-I4 will be presented, including the architecture overview, simulation results, preliminary measurements and a global design flow.

Summary

The FE-I4 project is a complex mixed-signal SoC, whose basic function is to record the time stamp and the charge of all hit pixels and transfer it outside of the chip. The charge due to the hits are brought to the chip through the coupled external sensors with negative charge collection. A major differentiator compared to its predecessor (FE-I3) is that it has been designed using the 130 nm CMOS technology. Not only this technology has smaller features sizes, it also enables better radiation hardness of the transistors from the characterized standard cell libraries. In addition, the technology allows a lower operating power while higher rate becomes also easily achievable. The pixel area contains 336 rows that are split with 80 columns on 50μ pitch. Different to the FE-I3 predecessor, the columns are split into 2 by 2 pixel regions to enable better luminosity and address the problem of a timewalk. Each region contains therefore four analog front ends which share memory and digital block. The analog front end is built as a two stage (pre)amplifer architecture and includes the discriminator with an adjustable threshold. The output is synchronized with the external clock of 40 MHz, so that all region operations are synchronous. Each synchronized discriminator output is further processed by applying a digital cut on the time over threshold (TOT). Hits smaller than a certain TOT (programmable between 1 and 3 clock cycles) are classified as “small hits” while others are classified as “large hits”. Only the large hits and at least one large hit in a given region will start the read-out process. The complex digital processing circuitry at the end of columns and the chip takes care that the data is properly read out. All digital circuits are designed using the standard cell libraries and are isolated from the substrate using the deep well structure (T3 isolation well) inherent to the manufacturing process. The chip size is 2cm×1.9cm and operates at 1.2V and 1.4V nominal supply for digital and analog part of the chip, respectively. The DC leakage current tolerance is 100nA, the radiation tolerance 250MRad, while the maximum charge amounts to 100 000 electrons. The basic performance of the analog front end has been validated with small prototypes irradiated to 200 MRad.
The chip architecture has been organized in a modular fashion to facilitate the multi-site nature of the project, i.e., where the design team have been scattered throughout the world. State of the art tools from the appropriate commercial EDA vendors have been used, while applying current industrial standard practices to set up and execute the design flow and perform the sign off. Since the FE-I4 chip will be undergoing high volume production, an appropriate Deign-for-Test (DfT) strategy has also been devised. The first application of the chip is expected to take place in the Insertable B- Layer (IBL) upgrade. Another application is scheduled to be with the outer pixel layers for the SLHC.

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