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# Upgrading the ATLAS Level-1 Calorimeter Trigger using Topological Information

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The ATLAS Level-1 Calorimeter Trigger (L1Calo) is a fixed latency, hardware-based pipelined system designed for operation at the LHC design luminosity of 10^34cm-2s-1. Plans for a several-fold luminosity upgrade will necessitate a complete replacement for L1Calo (Phase II).
But backgrounds at or near design luminosity may also require incremental upgrades to the current L1Calo system (Phase I). This paper describes a proposed upgrade to the existing L1Calo to add topological algorithm capabilities, using Region of Interest (RoI) information currently produced by the Jet and EM/Hadron algorithm processors but not used in the Level-1 real-time data path.

## Summary

The ATLAS Level-1 Calorimeter Trigger (L1Calo) is a fixed latency hardware-based pipelined system. The real-time data path includes the preprocessor that conditions and digitizes analog tower sums, and two parallel digital algorithm processor subsystems that separately produce detector-wide EM/hadron cluster and Jet/Energy-sum results to send to the Central Trigger Processor, which produces the final Level-1 trigger decision. L1Calo was designed to cope with the LHC design luminosity and a complete replacement is being designed for the several-fold luminosity upgrade planned for the LHC.

Recent simulations suggest pile-up may pose challenges to the L1Calo even near the design luminosity, and trigger algorithms may need to be augmented to reduce rates and improve selectivity even before the current L1Calo is replaced. A promising solution is to add topological algorithms based on the Region of Interest (RoI) information currently produced in the algorithm processors for use in Level-2, but not in the Level-1 real-time data path. By modifying the firmware in the existing algorithm processor modules and running the existing backplane merger connections at a higher clock speed, this information can be included in the real-time data path and processed in real time.

The result-merging boards in the current system must be redesigned to include more modern programmable logic and high-bandwidth optical data links. These boards will initially retain backward compatibility with the current system, but also enable topological algorithm processing to be added, either among the merging boards themselves or in a new, separate topological processor subsystem (TP). The proposed upgrade may also require firmware changes in the CTP to increase the number of trigger inputs available.

Tests with the current L1Calo backplane and algorithm processor boards have shown the feasibility of expanding the real-time data path bandwidth. Monte Carlo studies of the proposed topological algorithms are in progress, as is technical specification of the combined merger/ topological processor stage. Modifications to the current Level-1 Calorimeter Trigger system shall be reversible and backward compatible, and allow early deployment and parasitic testing of some components of the Phase II system.

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