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A 10Gb/s Serial Communication Transceiver in 0.13µm CMOS for a 2m Micro Twisted-Pair Cable

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Pixel chips generate a large amount of data. In the foreseen application, the data has to be transported off chip via a micro twisted-pair cable. Because of the low bandwidth of the cable, equalization is needed. Pulse-width modulation turns out to be the best equalization method at the transmitter side. However, at 10Gb/s the eye-opening at the receiver side is very sensitive to the exact value of the pulse-width. This sensitivity can be significantly improved by using an on-chip parallel RC combination in series with the transmitter. A demonstrator chip in 0.13µm CMOS is designed to prove the concept.

Summary

Pixel chips for future applications produce a virtually infinite amount of data. For imaging, there is a need for more frames per second, while high energy physics experiments will run at a higher luminosity, meaning more hits per second. All this data has to be transported off the pixel chip.

For the upgrade of the LHCb experiment at CERN (VeloPix chip), the expected link speed is about 10Gb/s. Because of the extreme radiation dose, electrical signals between the pixel modules and the optical modules will be transmitted over micro twisted-pair cables with a length of one to two meters. The bandwidth of these micro twisted-pair cables is severely limited. The transfer function for a characteristically terminated cable of 2m has a loss of 42dB at 5GHz. Therefore, without using equalization techniques, a data rate of 10Gb/s is not possible.

In order to find the best equalization method for the micro-twisted pair cable, different equalization techniques were analyzed. In order to do this, first, the s-parameters of a typical cable were measured. From these, the parameters of a transmission line model were derived. This model includes skin effect and dielectric loss. Using this model, the transfer function of the cable can be calculated. From the transfer function, the impulse response and symbol response are calculated. With the symbol response, the eye-opening of the eye-diagram at the receiver side is determined [1]. In this way, the eye-opening for different equalization techniques can be found.

Pulse-Width Modulation (PWM) turned out to be the best equalization technique at the transmitter side. With this technique, a logical one is transmitted as *+½Vout for a period of pwm*TS and *-½Vout for a period of (1-pwm)*TS. TS is the symbol time, pwm the pulse-width parameter and Vout is the output swing. A logical zero is transmitted as the inverse of the logical one. For a data rate of 10Gb/s, the pwm parameter should be close to 0.5.

Unfortunately, for a driver with low output impedance, the eye-opening turns out to be very sensitive to the exact value of the pwm parameter. Small deviations from the nominal value already close the eye. To make the design more robust, an on-chip parallel RC combination is placed in series with the transmitter. The RC constant is matched to the cable characteristics. The result of this RC filter is that the eye at the receiver side stays open for a much wider range of the pwm parameter. Spread of the R and C values has little impact. Another advantage of the RC filter is that the transmission is less sensitive to bondwire inductance.

A chip was designed in a 0.13µm 1.2V process. Current-Mode Logic (CML) cells were used throughout the design to meet the speed requirements. Some critical blocks use inductive peaking. In the receiver, high gain is achieved by a cascade of CML buffers. A DC feedback loop is used to compensate for offset. The area of the transmitter is 0.35mm2 and the area of the receiver 0.10mm2. The power consumption is 60mW for the transmitter and 16mW for the receiver.

[1] D. Schinkel, E. Mensink, E. A. M. Klumperink, E. van Tuijl, and B. Nauta, "A 3-Gb/s/ch transceiver for 10-mm uninterrupted RC-limited global on-chip interconnects," IEEE J. Solid-State Circuits, vol. 41, no. 1, pp. 297-306, Jan. 2006.

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