Components for the Control System of a Future Pixel Detector

TWEPP 2010 – Topical Workshop on Electronics for Particle Physics

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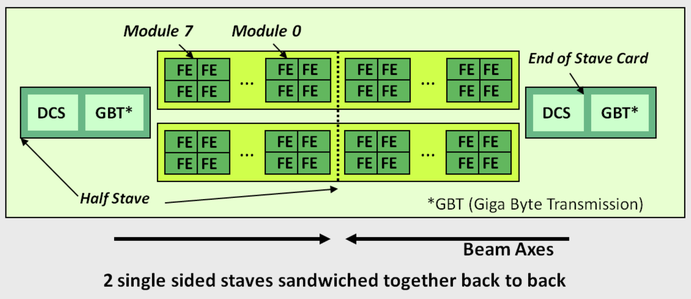
Upgrades of the LHC and the ATLAS experiment will include a new pixel detector. To operate a future pixel detector, a completely new detector control system (DCS) is needed, that is embedded in the pixel electrical systems. Next to high reliability the requirements for the detector control system are less usage of material and cable and radiation hardness to always guarantee a save operation of the experiment. To meet these requirements we propose a DCS network which consists of a DCS chip and a DCS controller. With a special focus on the communication interface, radiation hardness and robustness against single event upsets, we present the development of the first prototypes.

ATLAS Pixel Detector at the sLHC

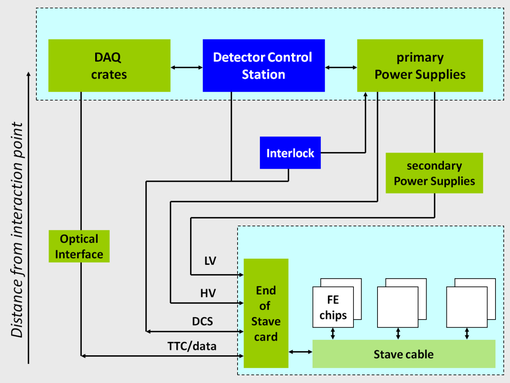
- A completely new design is necessary
- Detector modules are mounted on staves or disks
- Detector layout:
  - 2 Layer insertable in the barrel's most inner part
  - Up to 3 fixed outer layers + up to 5 disks/endcap
- Ca. 6000 detector modules
- $|\eta| \leq 2.5$
- Pixel size of the outer layers: (50 x 250) μm^2
- Radiation dose
  - 570 MRad
  - $2.4 \cdot 10^9$ particles $\cdot cm^{-2} \cdot s^{-1}$ (SEE flux)

STAVE of the outer Layers (2,3 & 4)



2 single sided staves sandwiched together back to back

Pixel Electrical System



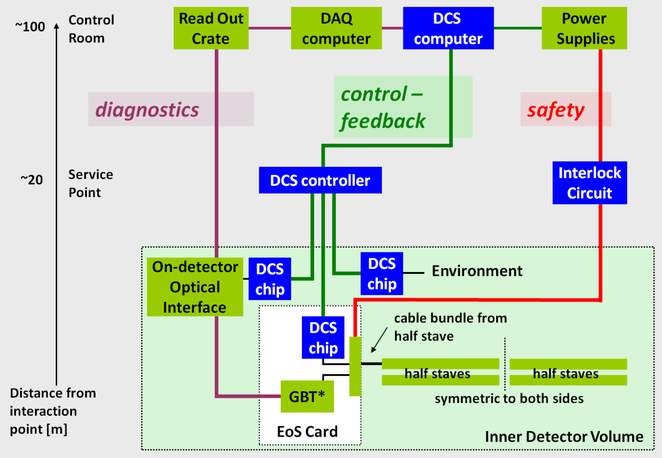
- **TTC (Trigger Timing Command) and readout data chain:**
  - 40-80 Mbps for TTC
  - Up to 320 Mbps for data
  - Electrical signals between FE chip and optical interface
  - Optical data between optical interface and DAQ crates
  - Outer layers will use GBT chip set (CERN microelectronics group)
- **Power Supplies:**
  - Depletion voltage for sensors
  - Low voltage (LV) for front end electronics: primary and secondary power supplies
  - 2 LV powering schemes under discussion
    - Serial
    - Parallel (using DC-DC converters)
  - Further supplies for End-of-Stave (EoS) card and optical interface
- **DCS (Detector Control System)** oversees detector modules, EoS card, optical interface and monitors the environment. Its requirements are:
  - High reliability
  - Radiation hardness
  - Low material volume

TTC, data, powering and DCS lines are organized per half barrel stave/disk sector.

DCS Architecture

The DCS architecture consists of three independent paths:

- **Safety**
  - Always on
  - Highest reliability
  - Low granularity
  - Hardwired interlock system
- **Control & Feedback**
  - For all use cases
  - High reliability, independent of data path
  - Steering and monitoring of modules, end of stave card, optical interface
  - Per detector module or half stave
- **Diagnostics**
  - On request during calibration
  - Per front end chip
  - Data is merged into data path



DCS Chip

Requirements:

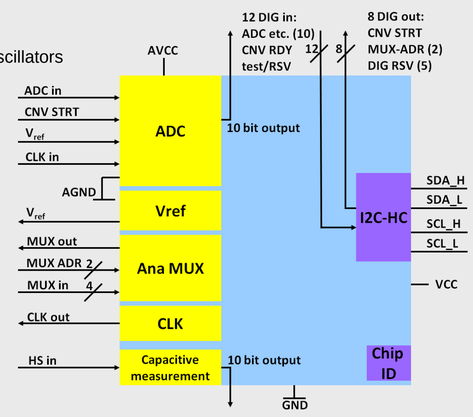
- Radiation hard at innermost layer of the Pixel Detector
- As few lines as possible
- Communication interface
- Low power consumption (for operation without cooling)
- Suitable for serial and parallel powering concept
- 35 ADC channels
- 2 16-bit counters + 2 identical working RC oscillators for capacitive humidity measurements
- 17 digital outputs

Connection to outer world:

- Power, data and clock will have separate lines
- Data is sent via a differentially wired I2C bus to master located at service point

Prototyping:

- Analog blocks:
  - 10 bit differential ADC
  - 2 identical working RC oscillators
  - V_{ref} for ADC
- Digital blocks:
  - Chip ID
  - I2C-HC slave



DCS Controller Chip

Requirements:

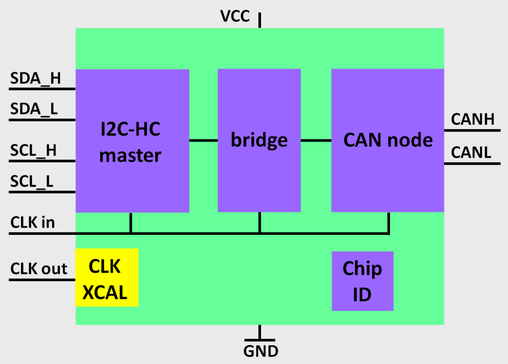
- Radiation hard
- As few lines as possible
- CAN node
- Master of the DCS chip interface
- Bridge between both interfaces

Connection to outer world:

- Power, data and clock will have separate lines
- DCS chip data is sent to the counting room via CAN

Prototyping:

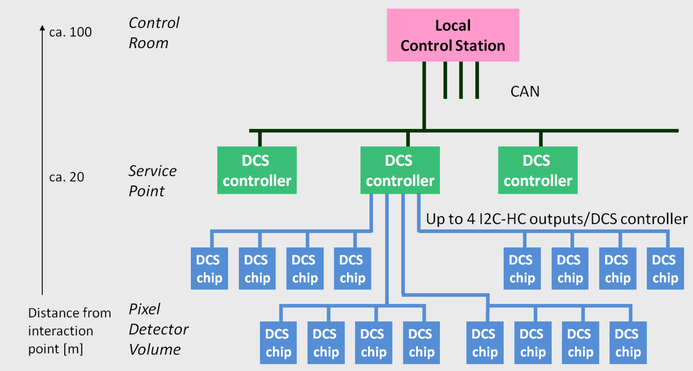
- Analog block:
  - Clock
- Digital blocks:
  - CAN node
  - I2C-HC master
  - Bridge
  - Chip ID



DCS Network

The DCS network is the control & feedback path. It is a compromise between highest possible reduction of cables and minimization of the risk to lose control of DCS items.

- Consists of DCS chip and DCS controller
- DCS chip located at the end of stave
- DCS controller located at a service point (20 m from the interaction point)
- 4 x 4 DCS chips are connected to one DCS controller
- DCS controller is connected to the control station in the counting room



CoFee1 Chip – A Prototype for the DCS Chip and the DCS Controller

The CoFee1 chip is a prototype for the digital blocks of the DCS chip and the DCS controller. Due to cost efficiency both cores were implemented in one chip. The implementation is designed to be radiation hard.

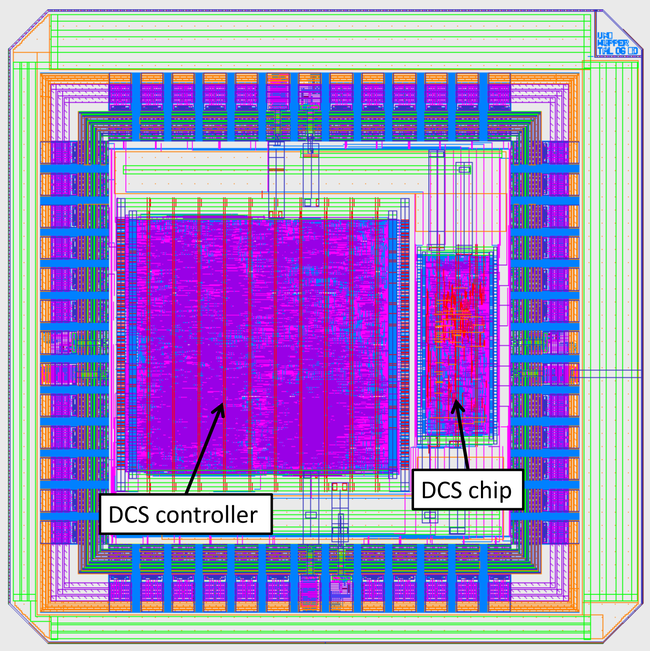
The DCS chip core features:

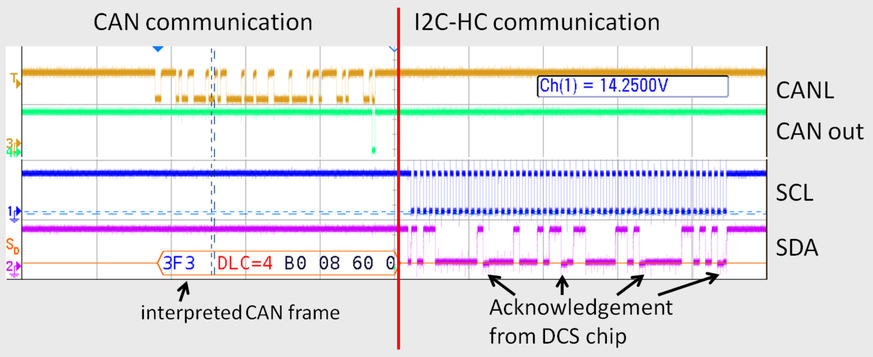
- I2C-HC slave, a standard I^2C interface extended by a (12, 8) Hamming code
- Registers with triple modular redundancy
- Inputs for ADC data
- 3 digital outputs
- 2 16-bit counters

The DCS controller core features:

- Standard CAN node
- I2C-HC master
- Bridge to translate between the interfaces
- Registers with triple modular redundancy

The CoFee1 Chip was submitted in June 2010 and will be produced in a 130 nm technology.





With the CoFee1 chip it will be possible to build the communication chain of the control & feedback path.

An example from an FPGA test can be seen above:

- The computers (in the counting room) send commands via CAN to the DCS controller core
- The DCS controller core reacts by sending commands to the DCS chip core via I2C-HC
- The DCS chip core acknowledges the reception of the commands and reacts accordingly

The control & feedback communication has been realized by implementing the DCS chip core and the DCS controller core.