Design of a Small-Dimension Low-Noise Dropout Regulator Built-in Monolithic Active Pixel Sensors (MAPS) for STAR Experiment

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Abstract: **An on-chip low dropout (LDO) regulator is presented, which provides the clamping voltage in monolithic active pixel sensors (MAPS) for the STAR experiment. By utilizing a buffer and a serial RC network, the regulator can achieve good stability, low power dissipation and low noise. Its output voltage is programmable by using a digital-controlled resistor. The proposed LDO regulator has been implemented in a 0.35 μm CMOS process. The die area is 327 μm × 119 μm. The power dissipation is 677 μW, and the output noise spectral densities at 100 Hz and 1 kHz are 222 and 74.8 nV/√Hz, respectively.**

Introduction:

The Solenoidal Tracker at RHIC (STAR) experiment is utilized to study the hot and dense nuclear matter created in high energy heavy ion collisions. In order to achieve high resolution vertex measurements, the upgrade heavy flavour tracker (HFT) will consist of three detectors, among which the PIXEL detector is the innermost and highest precision one (See Fig.1). MAPS find their applications on the implement of the PIXEL detector due to their advantages, such as integrating the sensors and readout electronics in the same substrate, offering high granularity and a thin sensitive volume. However, the upgrade brings new challenges to the design of MAPS. Based on the exiting detector, only a little space is left to place cables for the PIXEL detector. Indeed, the cables will degrade the radiation length, induce the noise and increase the heat loss. Therefore, all the reference and bias voltages in MAPS have to be generated on-chip by integrated regulators, except the power voltage (Vdd!) and ground voltage (Gnd!) (See Fig.2). As one of the important reference voltages, the clamping voltage is utilized for Correlated Double Sampling (CDS) operation (See Fig.3). Its value is 1.7 V-2.3 V. The objective of this poster is to present a low noise, low power dissipation and small dimension LDO, which is a fully on-chip to supply clamping voltage.

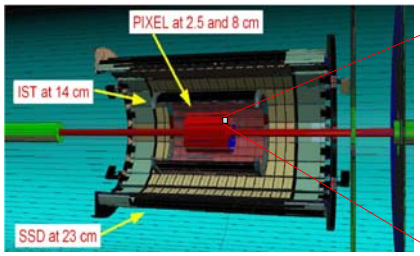


Figure 1

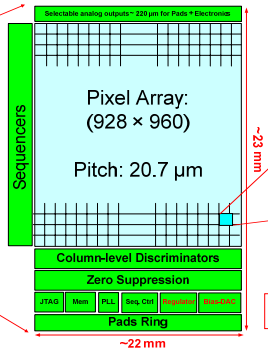
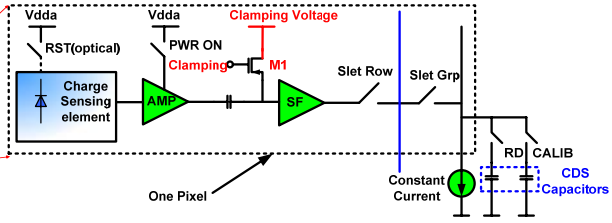


Figure 2



See the talk in this conference: Christine HU, "ULTIMATE: a High Resolution CMOS Pixel Sensor for the STAR Vertex Detector Upgrade "

Figure 3

The proposed LDO:

Design specification:

- Input voltage range is 2.7 V to 3.3 V.
- Output voltage is 1.7 V to 2.3 V (adjusted by JTAG registers).
- Load capacitance is larger than 0.5 nF which is estimated by layout parasitic extraction.
- External compensation components aren't allowed.
- PSRR is 50 dB.
- Noise spectral density is lower than 1μV/ √ Hz(@100-100 kHz)
- Power dissipation is less than 1 mW.

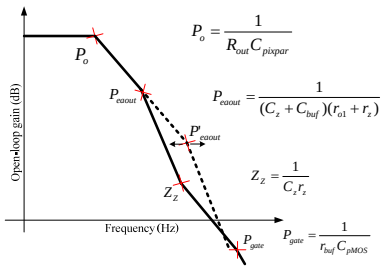


Figure 4. The AC response of the LDO before (dash line) and after (solid line) compensation

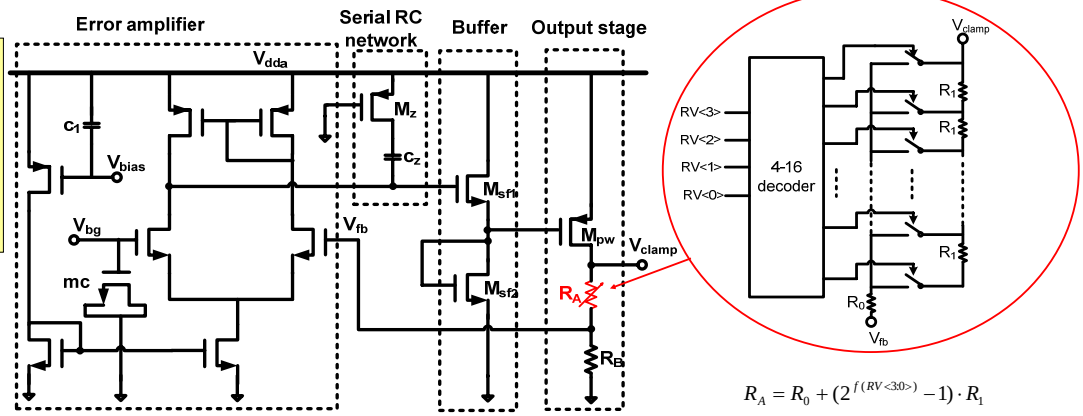


Figure 5

As shown in Fig.4, the pole located at the output of the error amplifier is cancelled by the zero induced by the serial RC (the transistor M_z operating in linear region and C_z in Fig.5).

The buffer stage can push the pole induced by pass transistor to high frequency. Moreover, the buffer decreases the dimension of pass transistor.

So the first dominant pole is located at the output. The smaller capacitance is employed to get good stability (See Fig.6, Fig.7).

This structure doesn't require extra current, power consumption and noise are low (See the Fig.8 and Table 1).

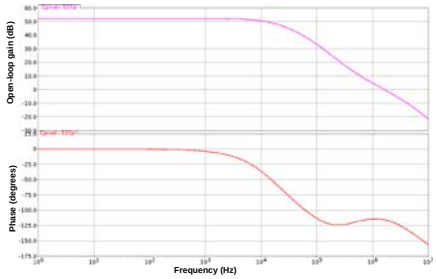


Figure 6

Simulate results:

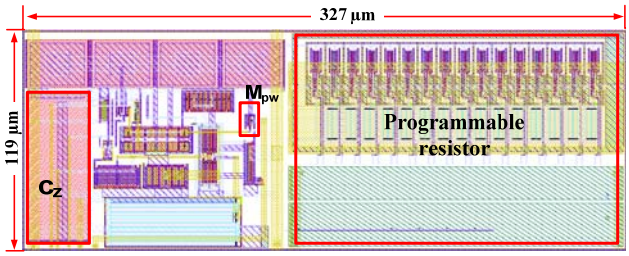


Figure 8

Table 1. The main performance parameters and the comparison with prior works

	Ref [1]	Ref [2]	This work
CMOS process	0.35 μm	0.13 μm	**0.35 μm**
Dropout voltage	200 mV	199 mV	**500 mV**
Supply voltage	3-6 V	3-4.5 V	**2.7-3.3 V**
Power (no load)	N/A	441 μW	**677 μW**
Output spectral noise density	N/A	338 nV/ √ Hz 100 Hz-5 kHz	**103 nV/ √ Hz 100 Hz-5 kHz**
Applications	DC-voltage transfer	RF SoC	**MAPS**

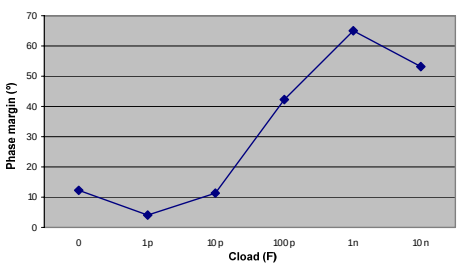


Figure 7

References

[1] K. Tsz-Fai and K. Wing-Hung, "A stable compensation scheme for low dropout regulator in the absence of ESR," in Solid State Circuits Conference, 2007. ESSCIRC 2007. 33rd European, 2007, pp. 416-419.

[2] K. Ka Chun and P. K. T. Mok, "Pole-zero tracking frequency compensation for low dropout regulator," in Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on, 2002, pp. IV-735-IV-738 vol.4.