Contribution ID: **34** Type: **Poster**

Design of a Small-Dimension Low-Noise Dropout Regulator Built-in Monolithic Active Pixel Sensors (MAPS) for STAR Experiment

Thursday 23 September 2010 16:00 (2 hours)

This paper presents an on-chip low dropout (LDO) regulator which provides the clamping voltage in monolithic active pixel sensors (MAPS) for STAR experiment. By utilizing a buffer and a serial RC network, the regulator can achieve good stability, low power and low noise. Its output voltage is programmable by using a digital-controlled resistor. The proposed LDO regulator has been implemented in a 0.35 μm CMOS process. The die area is 327 μm × 119 μm. The power dissipation is 600 μW, and the output noise spectral densities at 100 Hz and 1 kHz are 222 and 74.8 nV/√Hz, respectively.

Summary

The Solenoidal Tracker at RHIC (STAR) experiment is utilized to study the hot and dense nuclear matter created in high energy heavy ion collisions. In order to achieve high resolution vertex measurements, the upgrade heavy flavour tracker (HFT) will consist of three detectors, among which the PIXEL detector is the innermost and highest precision one. MAPS find its application on the implement of the PIXEL detector due to its advantages, such as integrating the sensors and readout electronics in the same substrate, offering high granularity and a thin sensitive volume. However, the upgrade brings new challenges to the design of MAPS. Based on the exiting HFT, little space is left to place cables for the PIXEL detector. If it is possible, the cables worsen the material budget, induce the noise and increase the heat loss. Therefore, the pads of MAPS must be as few as possible. The reference and bias voltages have to be generated on-chip by integrated regulators. In low-consumption MAPS, the clamping voltage is a pixel-level reference voltage for the coupled-double-sampling (CDS) operation. It must be noiseless. Since the clamping voltage is connected to each pixel, the parasitic capacitance will be extremely large for a large pixel array. For example, the capacitance value is up to 0.5 nF for 576 × 136 pixels. With such a load condition and low-noise requirement, the stability of the regulator becomes a big challenge. Moreover, no external passive components can be approved for frequency compensation. Consequently, an application specific regulator should be developed.

The linear LDO regulator is widely used due to its low noise, low power and compact die size. However, its stability should be carefully considered. Compared to other compensation schemes, three-stage architecture with a serial RC network is more suitable to the application of MAPS. As the second stage, a buffer implemented by a source follower is incorporated into the traditional two-stage LDO. The RC network is connected to the input of the buffer. In this structure, the first non-dominant pole is split into two poles by the buffer. One is pushed to high frequency and the other is canceled by the zero generated by the serial RC network. Since the compensation scheme requires less current, such a circuit can achieve both lower noise and lower power. This paper presents a LDO regulator based on this scheme, as well as a programmable output voltage to eliminate the influences of the process variations. Small-dimension compensation capacitor and power transistor are also achieved.

The proposed LDO has been designed and is being fabricated in AMS (Austria Micro Systems) standard CMOS 0.35 μm process. Its chip area is only 0.0389 mm². The LDO is verified by simulations. The output noise spectral densities at 100 Hz and 1 kHz are 222 and 74.8 nV/√Hz, respectively. The PSRR of the LDO is larger than 48 dB when the frequency is 150 kHz (-3dB frequency). The power dissipation with no loads is less than 600 μW. The measured results will be presented in the conference.

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Session Classification: POSTERS Session

Track Classification: ASICs