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Signal processing for High Granularity Calorimeter: amplification, filtering, memorization and digitalization

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A very-front-end chip dedicated to high granularity calorimeters has been designed and its performance measured. This electronics is composed of a low-noise Charge Sensitive Amplifier followed by a bandpass filter based on a gated integrator. This shaper performs intrinsically the analog memorization of the signal before its delayed digital conversion. The analog-to-digital conversion is obtained through a low-power 12-bit cyclic ADC. Measurements show a global non-linearity better than 0.1%. The ENC is evaluated to 1.8 fC, compare to the maximum input charge of 10 pC. The power consumption of a complete channel is limited to 6.5mW.

Summary

A very-front-end (VFE) electronics has been designed to fulfil requirements of next generation of electromagnetic calorimeters. The compactness of this kind of detector and its large number of channels (up to several millions) impose a drastic limitation of the power consumption of the VFE and its high level of integration. The electronic channel proposed is composed of a low-noise Charge Sensitive Amplifier able to amplified charge delivered by the silicon diode up to 10 pC. The dynamic range is improved using a bandpass filter based on a gated integrator (GI). The performance of this time-variant filter is compare by simulation with standard CRRC2 time-invariant filter. Studying their weighting functions, we show that this filter is more efficient than standard CRRC shaper, thanks to the time of integration which can be expand near the bunch interval time, whereas the peaking time of the CRRC shaper is limited to pile-up consideration. With a peaking time limited to 200 ns for the CRRC shaper and a time of integration up to 300 ns for the G.I., both serial and parallel noise indexes are reduced by about 30% with the G.I. filtering. Moreover, the G.I. performs intrinsically the analog memorization of the signal before its delayed digital conversion. The analog-to-digital conversion is obtained through a 12-bit cyclic ADC. This converter presents a good trade off between precision, speed and power consumption. Its integral non-linearity is within ±1.5 LSB with a power consumption limited to 1.5mW.

Measurements have been carried out on a prototype chip fabricated using a 0.35 µm CMOS technology. Measurements show a global non-linearity better than 0.1%. The Equivalent Noise Charge at the input of the channel is evaluated to 1.8 fC, compare to the maximum input charge of 10 pC. The power consumption of the complete channel is limited to 6.5mW.

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