

A Tezzaron-Chartered 3D-IC electronic for SLHC/ATLAS hybrid pixel detectors

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Hybrid pixels detectors featuring high spatial resolution, very good signal to noise ratio and radiation hardness are currently used in vertex detectors for High Energy Physics experiments. As technology shrinking reaches some limitations, a way to face challenges of ATLAS/SLHC future hybrid pixel vertex detectors is to use the emerging 3-D technologies. This talk presents the design and test of the 3-D chip prototypes realized with the Tezzaron-Chartered technology, as well as the design and test of read-out chip demonstrators 2-D using the same 0.13 μm Chartered technology. The 3-D variants are built by face to face, copper bonding of 2 electronics wafers. The first part includes all analog functions, and the second one is dedicated to digital. Finally, a sensor is foreseen to be connected to the read-out electronics by usual solder bumps. Design choices and test plans will be presented.

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