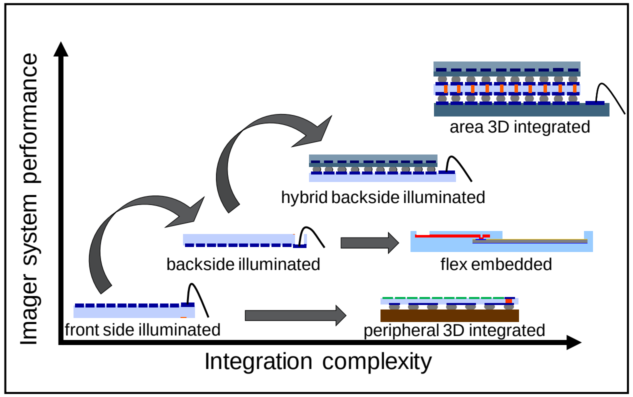
NEW INTERCONNECT TECHNOLOGIES FOR IMAGERS

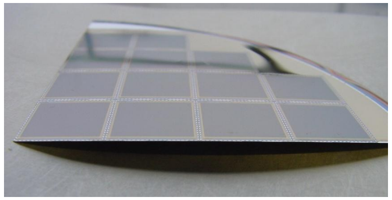
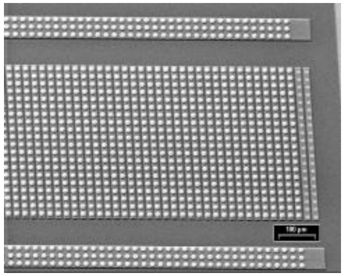
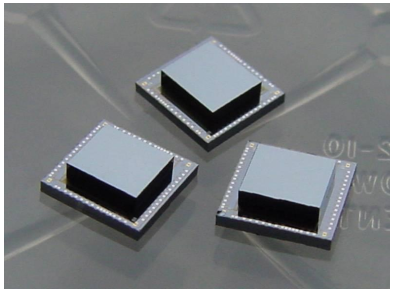
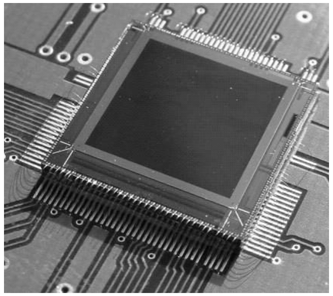
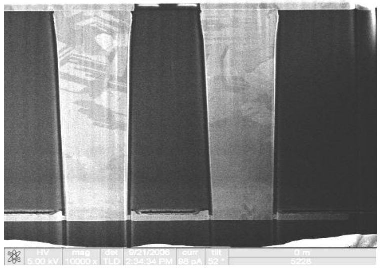
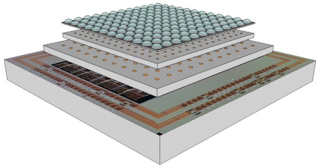
PIET DE MOOR

OUTLINE



- Introduction: imec vision & roadmap

- Technology components and results:
  - Frontside illuminated imagers
  - Backside illuminated imagers
  - Hybrid backside illuminated imagers
  - 3D integrated imagers
  - Flex embedded imagers

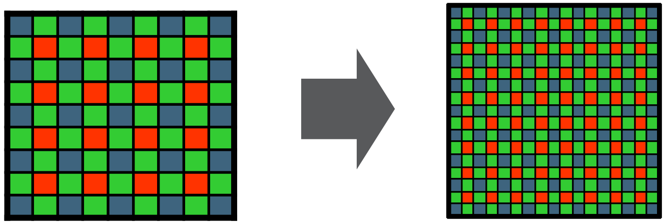
- Conclusion

IMAGING HISTORY

- Historical (r)evolution in radiation detection/imaging:
  - Single pixel → linear array → 2D array
- = thanks to:
  - Mother Nature: **Si** has a combination of unique properties
    - Right bandgap to detect visible light
    - Absorption of photons in a few micron thickness
    - The best/most practical semiconductor material
  - Development in **microelectronics fabrication technology**:
- Technologies:
  - Dedicated imager technology: **Charge Coupled Device (CCD)** – Nobel Prize 2009
  - **CMOS image sensors (CIS)** are taking over thanks to advantages of CMOS scaling: i.e. integration on electronics, low power, ...

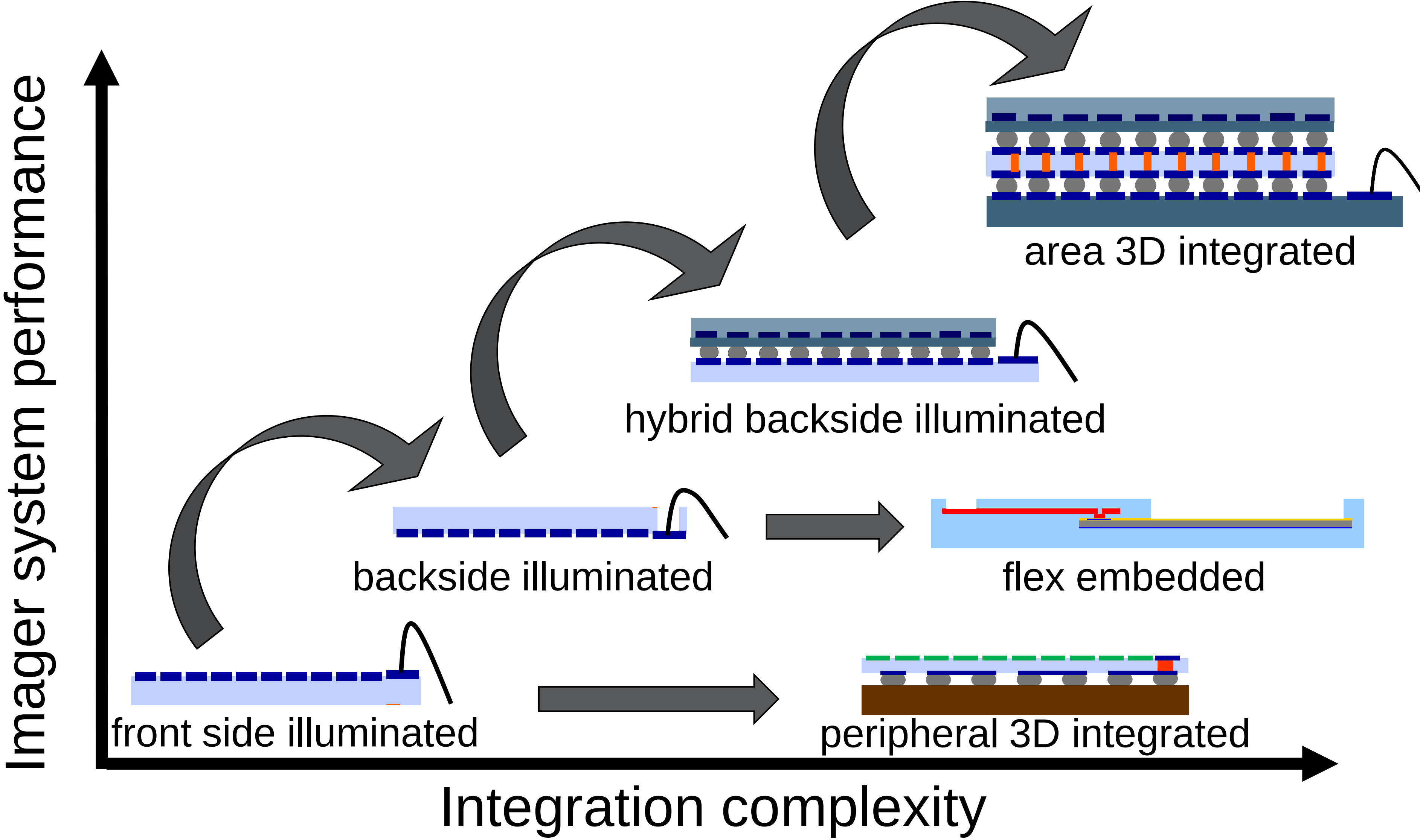
INTRODUCTION

- 2 imager roadmaps with a different approach:
  - Traditional roadmap: scaling to smaller pixels:
    - Equal chip size (or slightly smaller)
    - Higher resolution

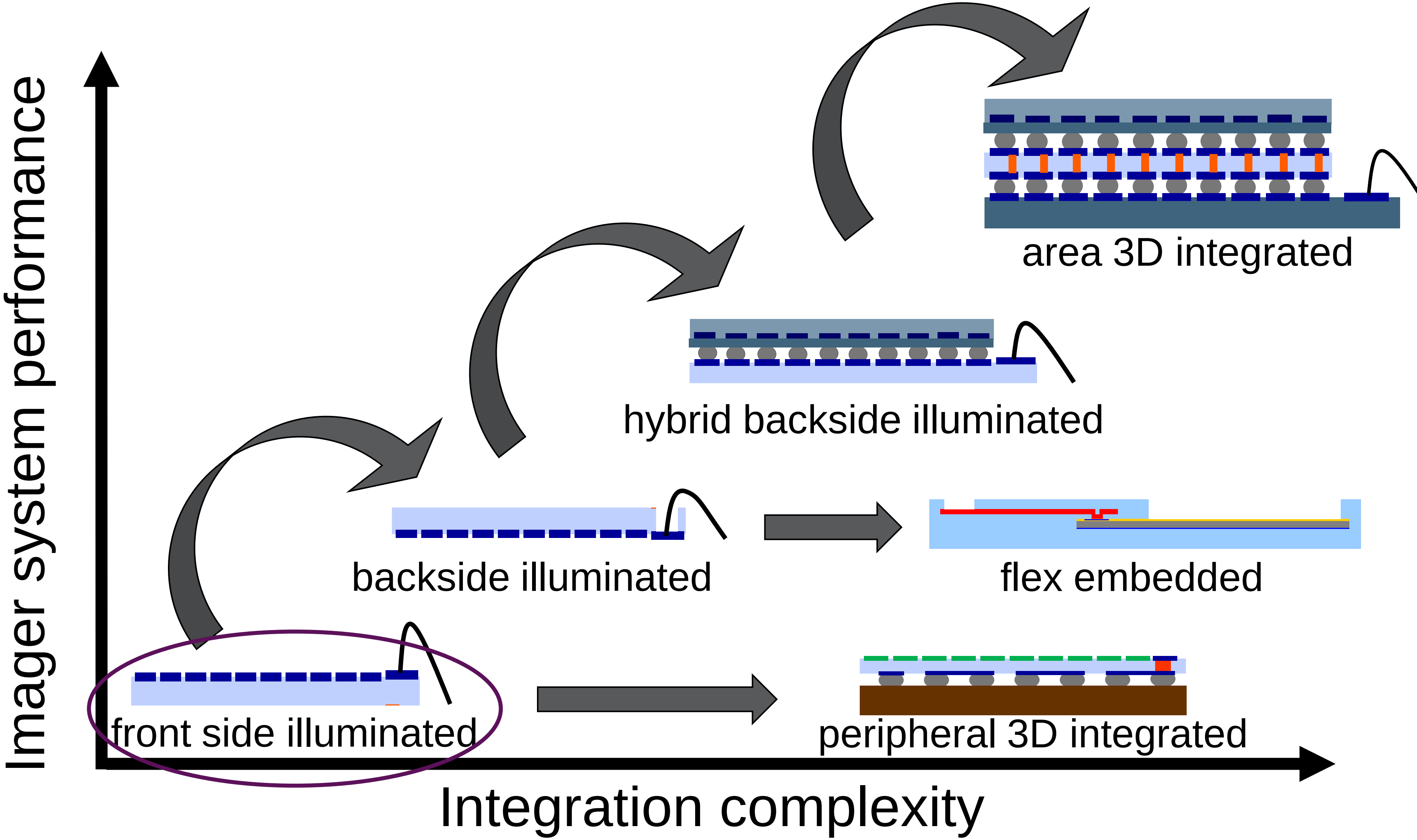


    - Lower sensitivity/pixel → backside illumination
  - IMEC Integration/packaging roadmap:
    - Backside illuminated → Hybrid → 3D integrated
    - Enables advanced imaging systems

IMEC VISION: ADVANCED IMAGER INTEGRATION



OUTLINE



Imager system performance

area 3D integrated

hybrid backside illuminated

backside illuminated

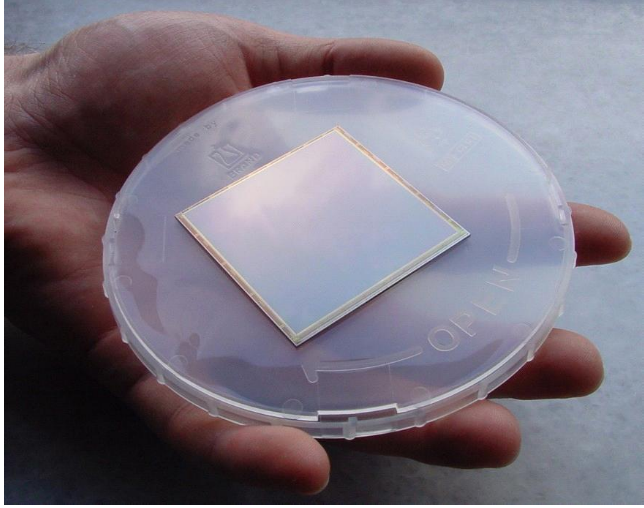
flex embedded

front side illuminated

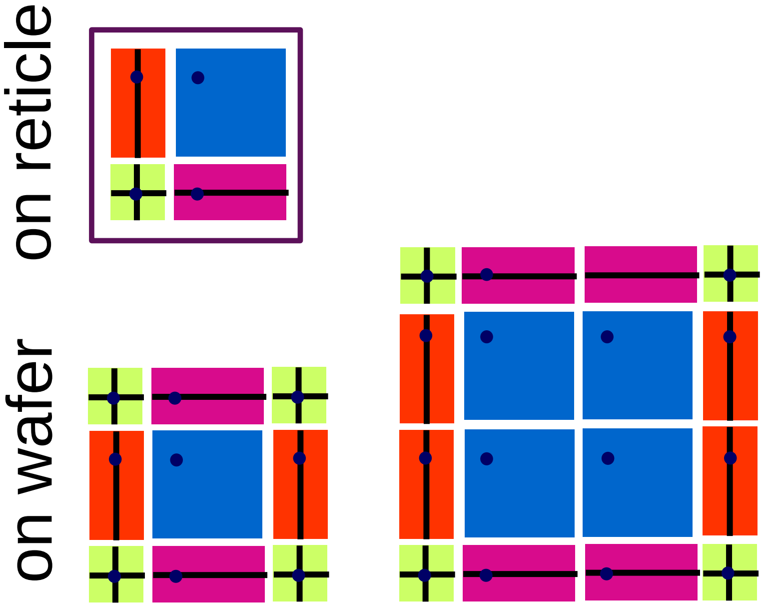
peripheral 3D integrated

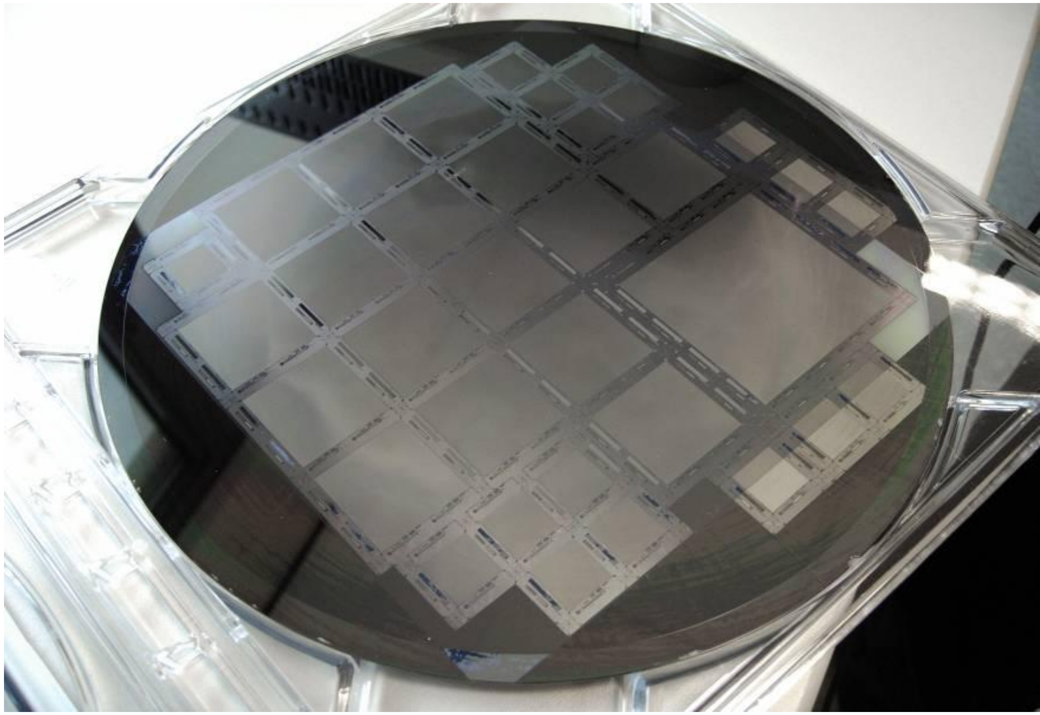
Integration complexity

LARGE AREA IMAGERS: STITCHING



- Stitching allows large area imagers:
  - Up to 1 imager per wafer
- Different imager sizes on one wafer demonstrated:
  - 12x12 mm^2, 25x25 mm^2 and 50x50 mm^2
- Application: e.g. X-ray

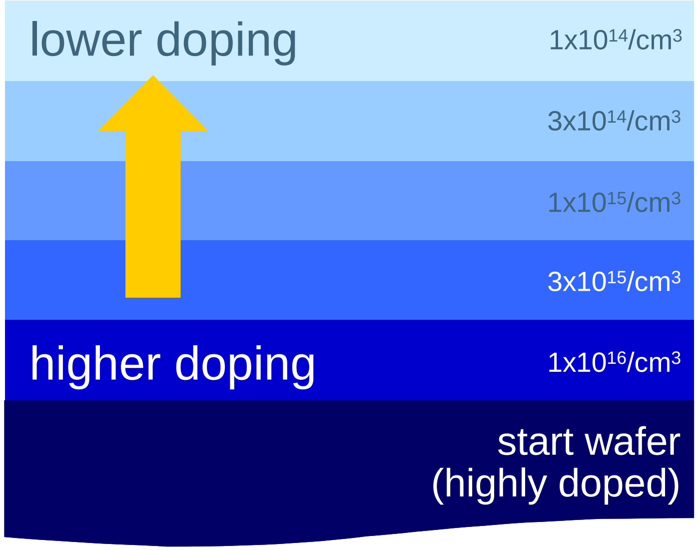


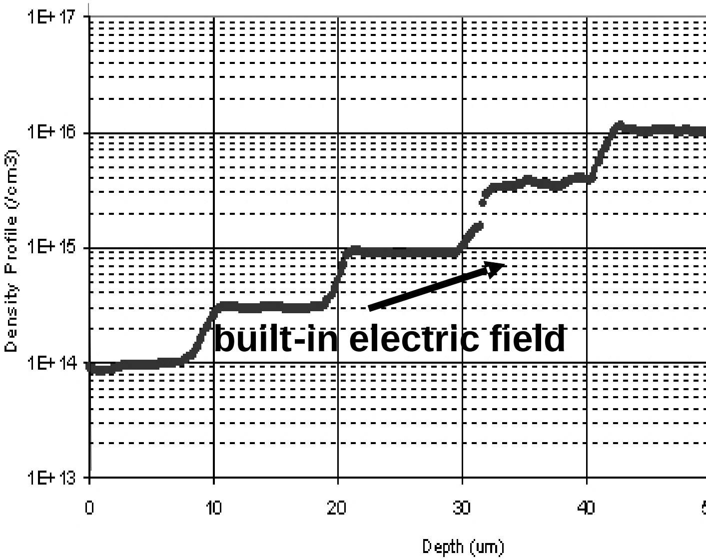


SPECIAL SUBSTRATES

- Epitaxial layers:
  - Thick:
    - Up to 50 um demonstrated
    - For detection of radiation penetrating deeper in Si
  - Graded dopant concentration
    - For directional carrier transport

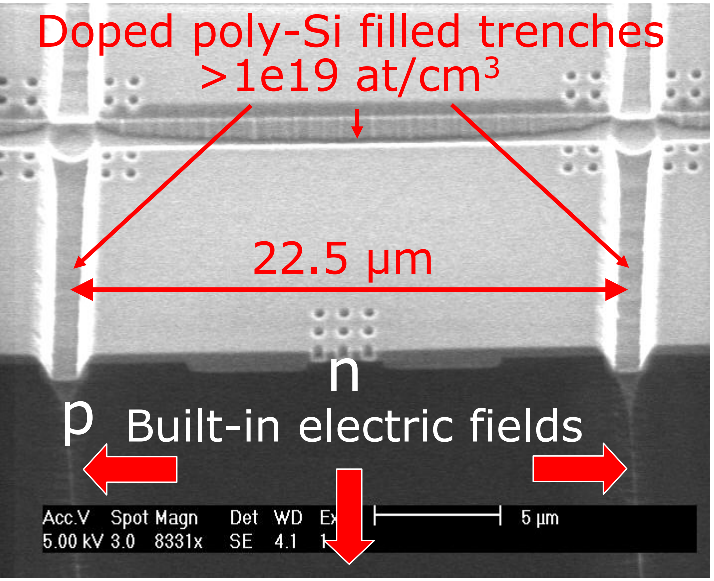
    = lower cross-talk
- High resistivity substrates:
  - Both n and p-type
  - Resistivity > 1kOhm.cm
  - Solution for chucking in imec fab
  - Application: fully depleted imagers for e.g. low cross-talk and X-ray direct detection





HYBRID BACKSIDE ILLUMINATED IMAGERS : TRENCHES FOR ZERO CROSS-TALK

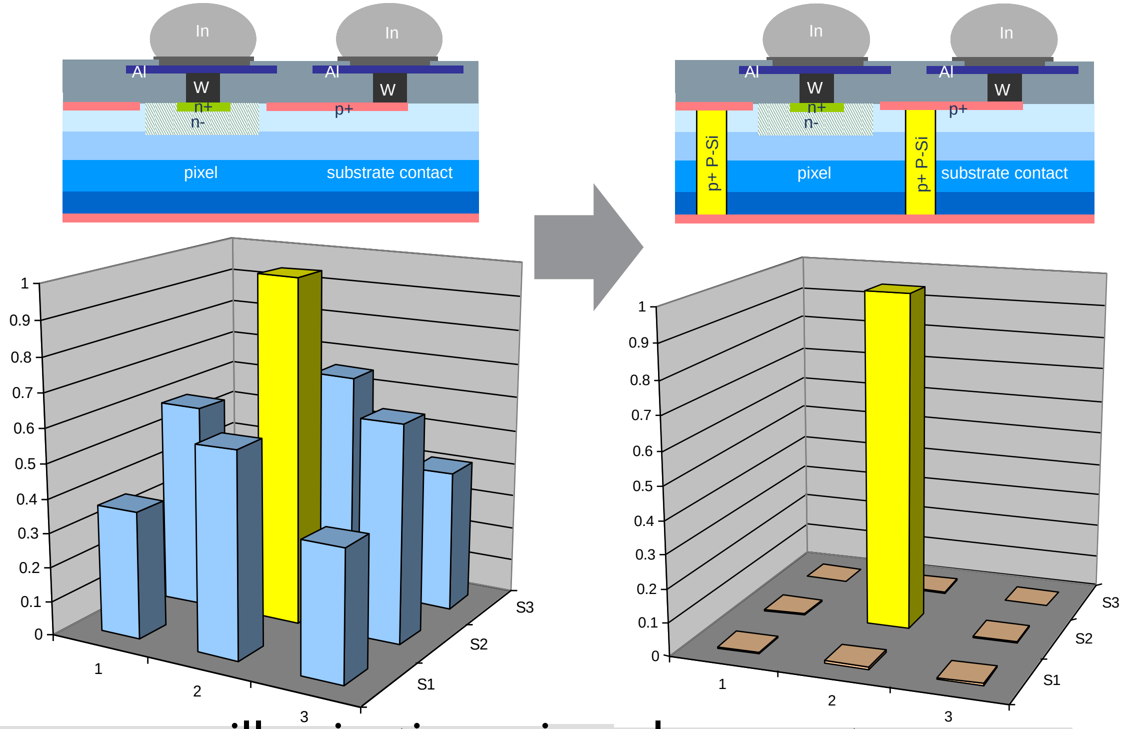
- Poly-Si doped trenches separating pixels:
  - Disadvantage: (limited) reduction in fill-factor
  - Advantage: no cross-talk
- Demonstrated using laser point source
- ongoing optimization: recovery of good charge collection & QE/


Doped poly-Si filled trenches $>1e19$ at/cm^3

22.5 µm

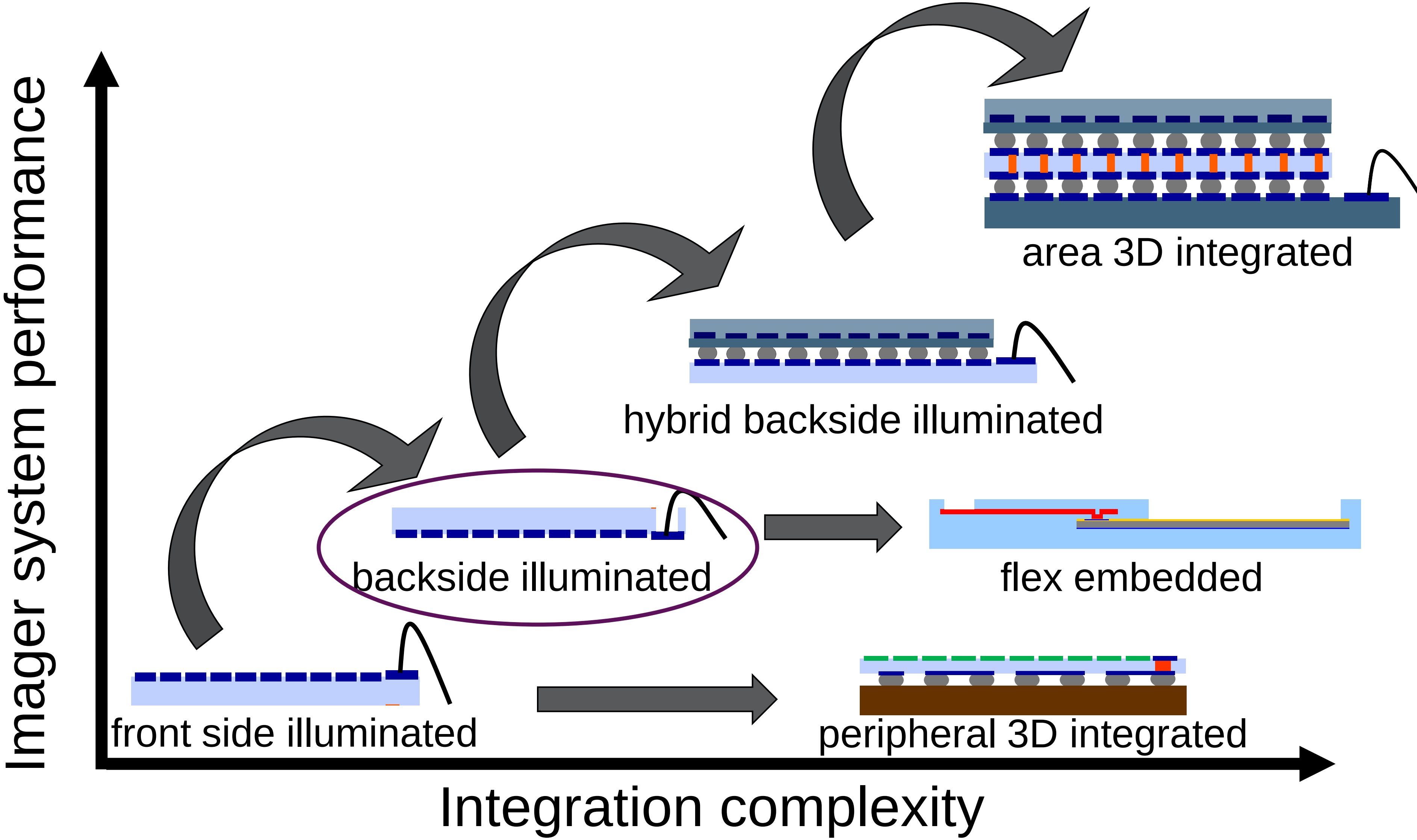
n

p Built-in electric fields

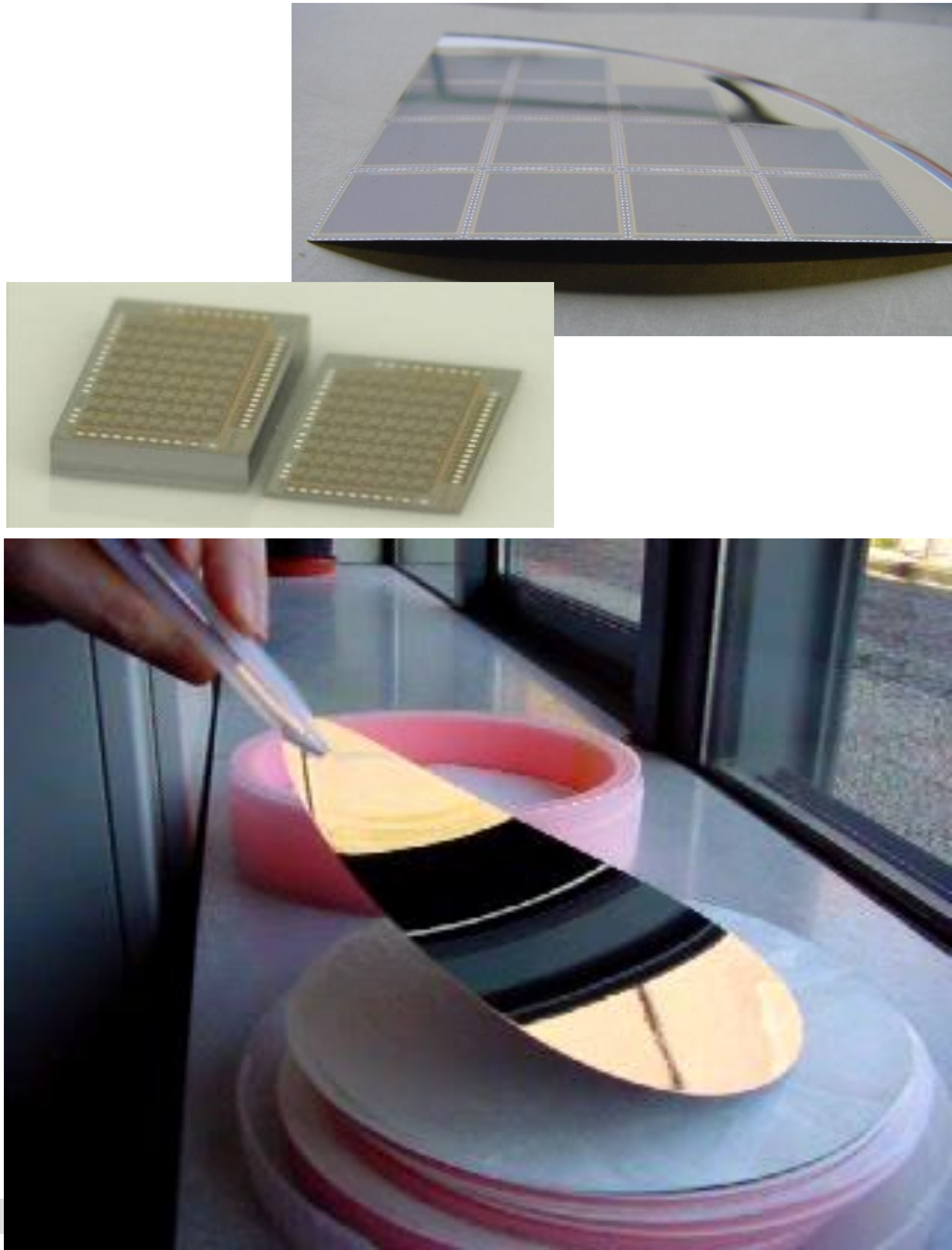


illumination using a laser spot

OUTLINE


area 3D integrated
hybrid backside illuminated
backside illuminated
flex embedded
front side illuminated
peripheral 3D integrated
Imager system performance
Integration complexity

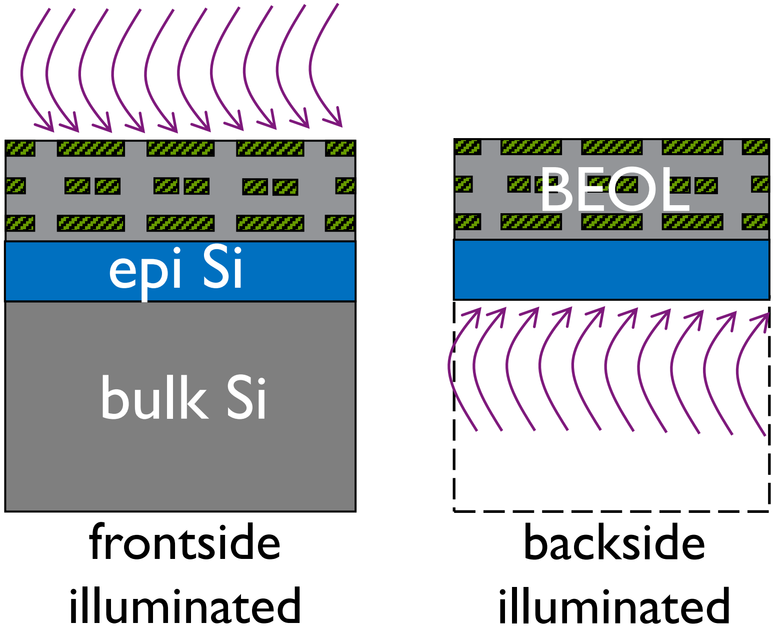
BACKSIDE ILLUMINATED IMAGERS: THINNING

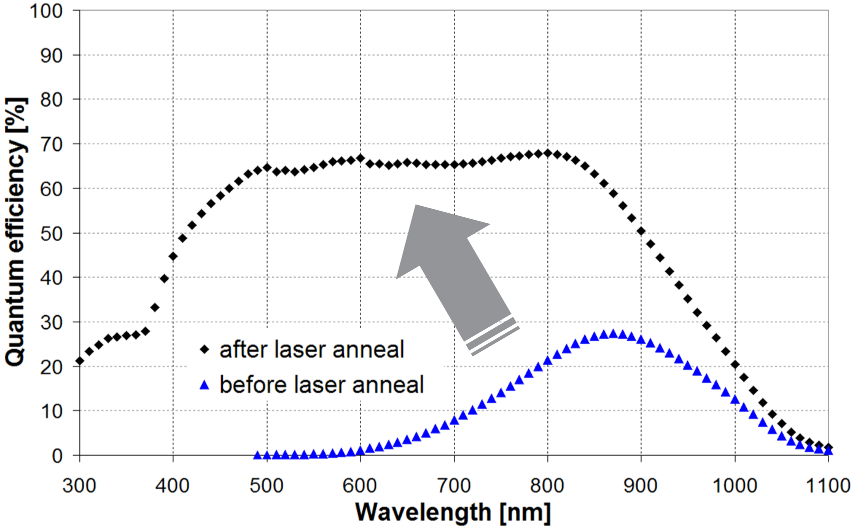


- Technology:
  - Course + fine grinding
  - Critical: thinning damage, impact on devices
- Wafer handling:
  - Very thin wafers (< 100 um): use of carrier wafers and temporary wafer (de-)bonding technology
- IMEC results:
  - Thinning down to 15 um
  - Total thickness variation ~ 2 um on 200 mm wafer

BACKSIDE ILLUMINATED IMAGERS:

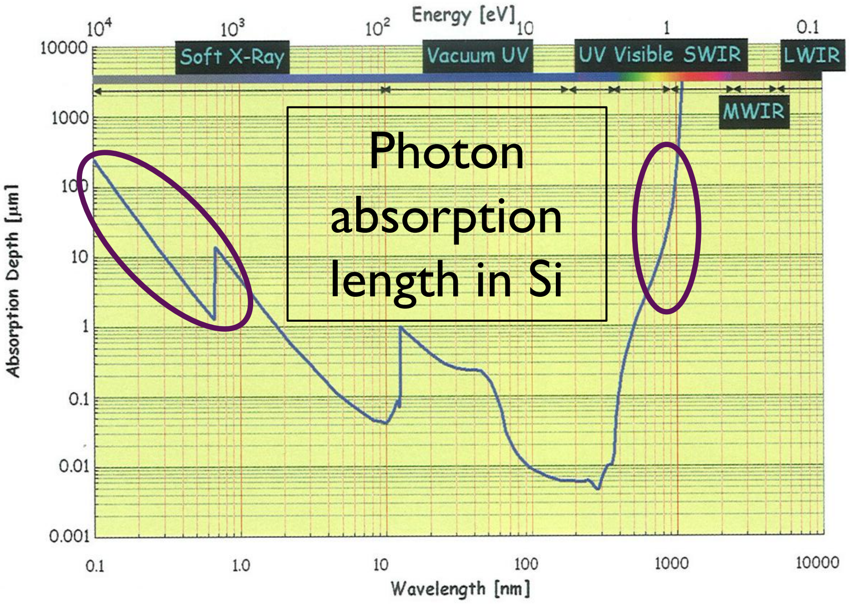
- Advantage: no dielectric/metal in radiation path:
  - 100% fill factor,
  - No QE loss
  - Broader wavelength range for radiation with shallow penetration (i.e. in UV)
- Technology:
  - Backside thinning + damage removal:
    - Combination of grinding and Si etch
  - Backside passivation of trapping centers:
    - High dose implant
    - Laser annealing (for low T budget)



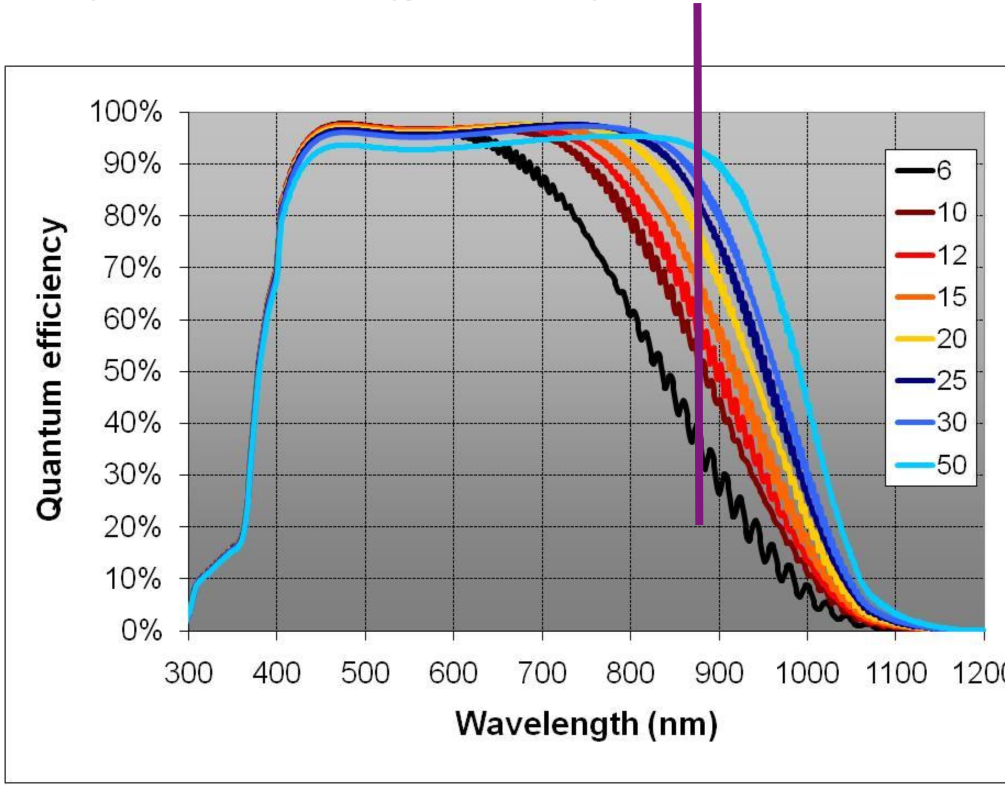


BACKSIDE ILLUMINATED IMAGERS: SENSITIVITY

- Reduced charge collection/QE for radiation with long absorption length
- Example @ 900 nm: 12 micron epi: 50% QE, 50 micron epi: 90% QE
- Similar challenge for X-ray detectection (λ < 1 nm, Energy > 1 keV)

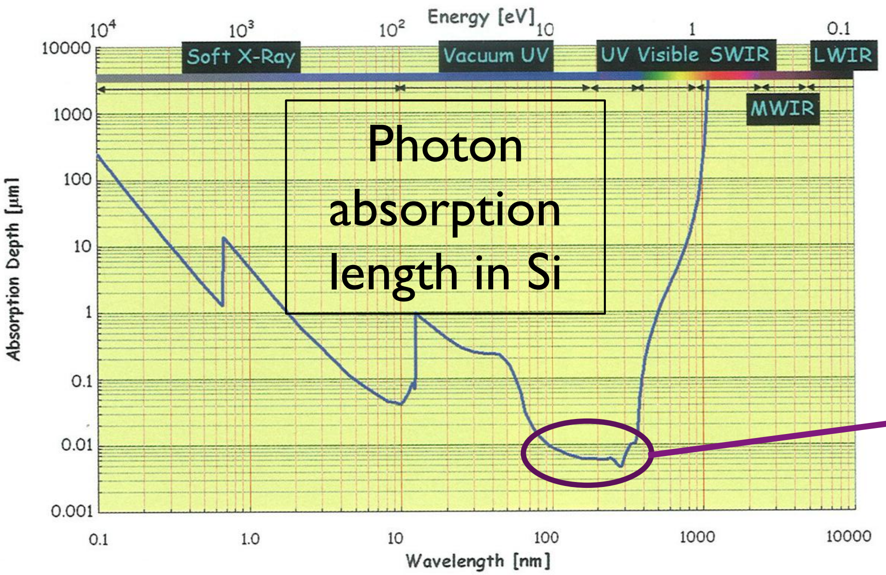


Photon absorption length in Si



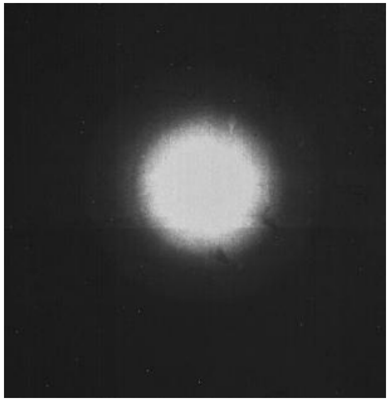
- Solution: thick epi or high resistivity substrates

BACKSIDE ILLUMINATED IMAGERS:
SENSITIVITY



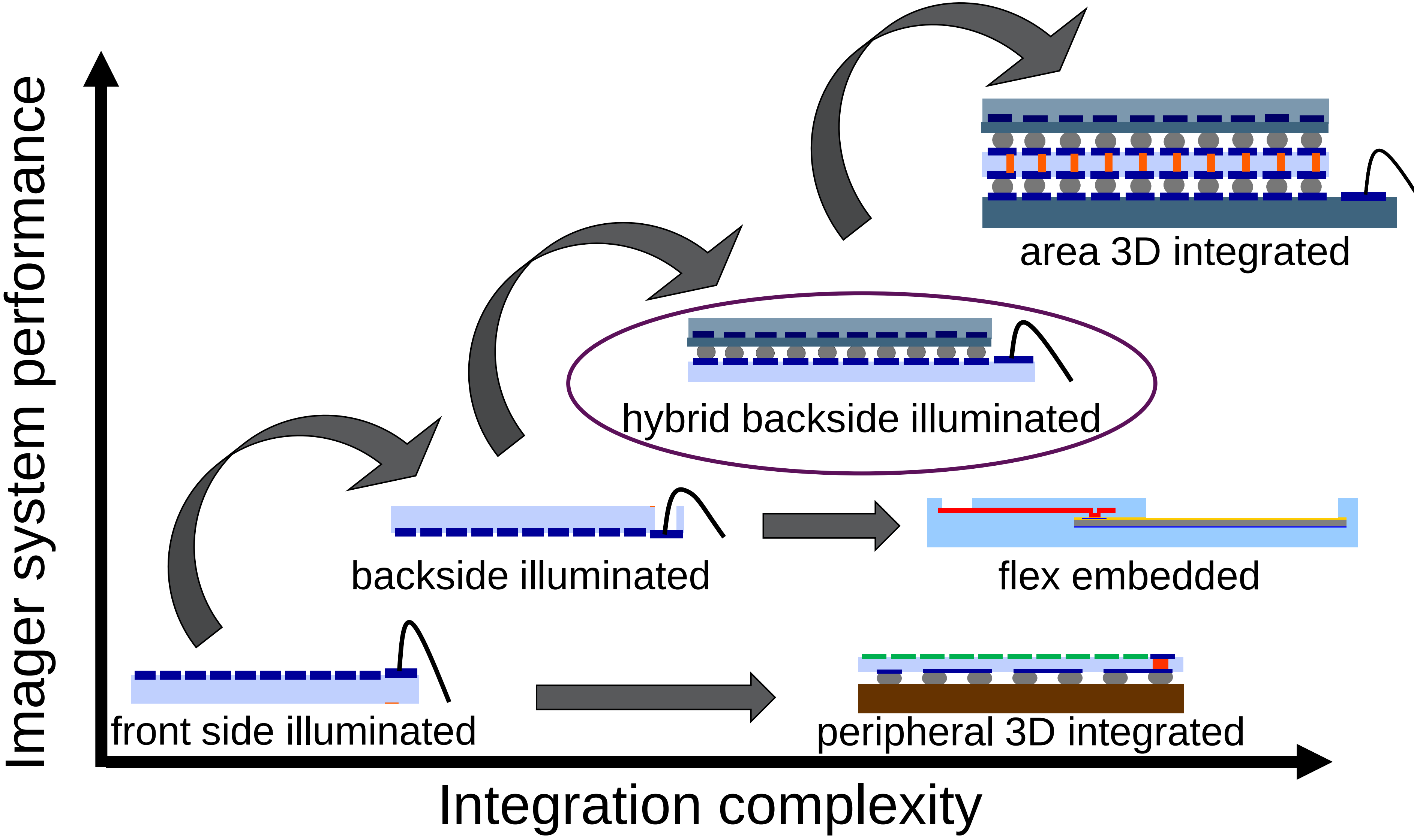
Photon absorption length in Si

@280 nm:
absorption length in Si is
~ 4 nm



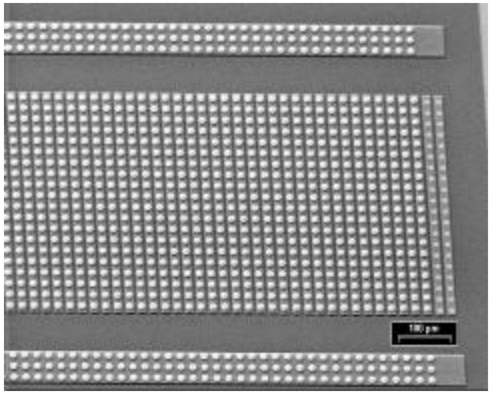
- Detection of radiation with short absorption length is a challenge:
  - Very short absorption length in dielectric materials (i.e. BEOL)
    - Solution: exposed Si, e.g. backside illumination
  - Very short absorption length in Si
    - Solution: very shallow passivation layer (< 10 nm), optimalization ongoing
- Example: (N)UV detection: sensitivity @ 280 nm demonstrated

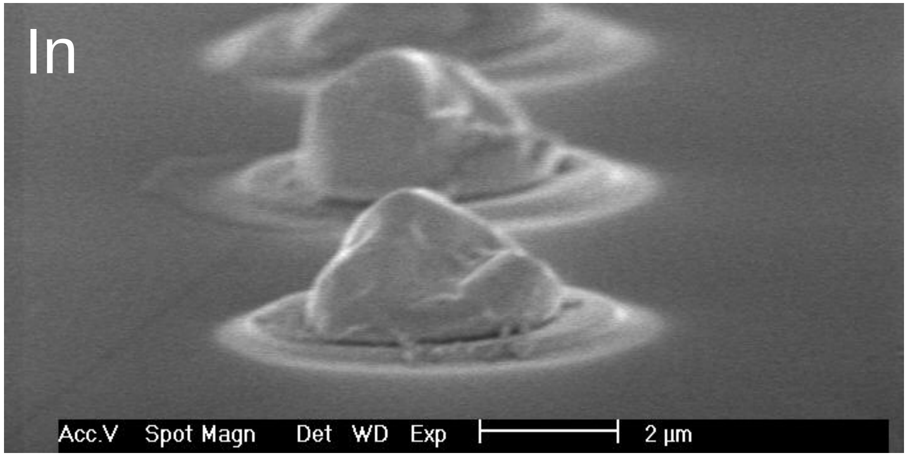
OUTLINE

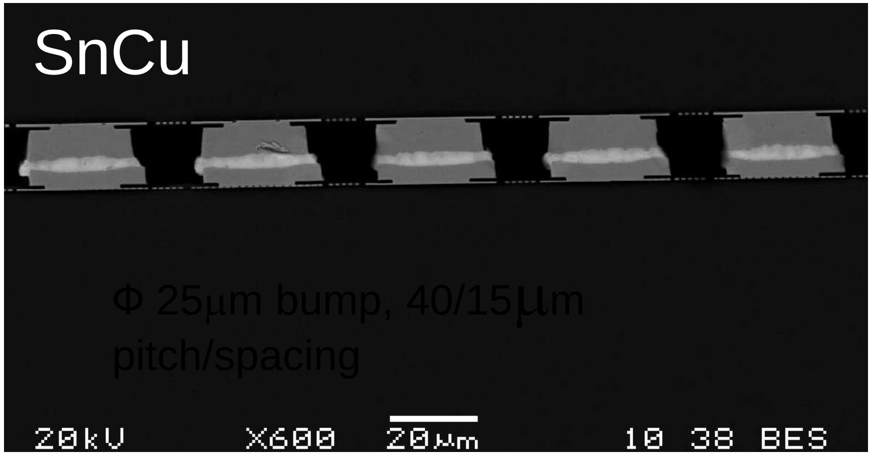

Imager system performance
area 3D integrated
hybrid backside illuminated
backside illuminated
flex embedded
front side illuminated
peripheral 3D integrated
Integration complexity

HYBRID BACKSIDE ILLUMINATED IMAGERS: HIGH DENSITY BUMPING

- In and CuSn microbumps:
  - Post-process at wafer level for both sides:
    - Under-bump metallization (UBM) & patterning
    - Solder deposition & patterning
  - Smallest pitch:
    - 20 um
    - 10 um under development



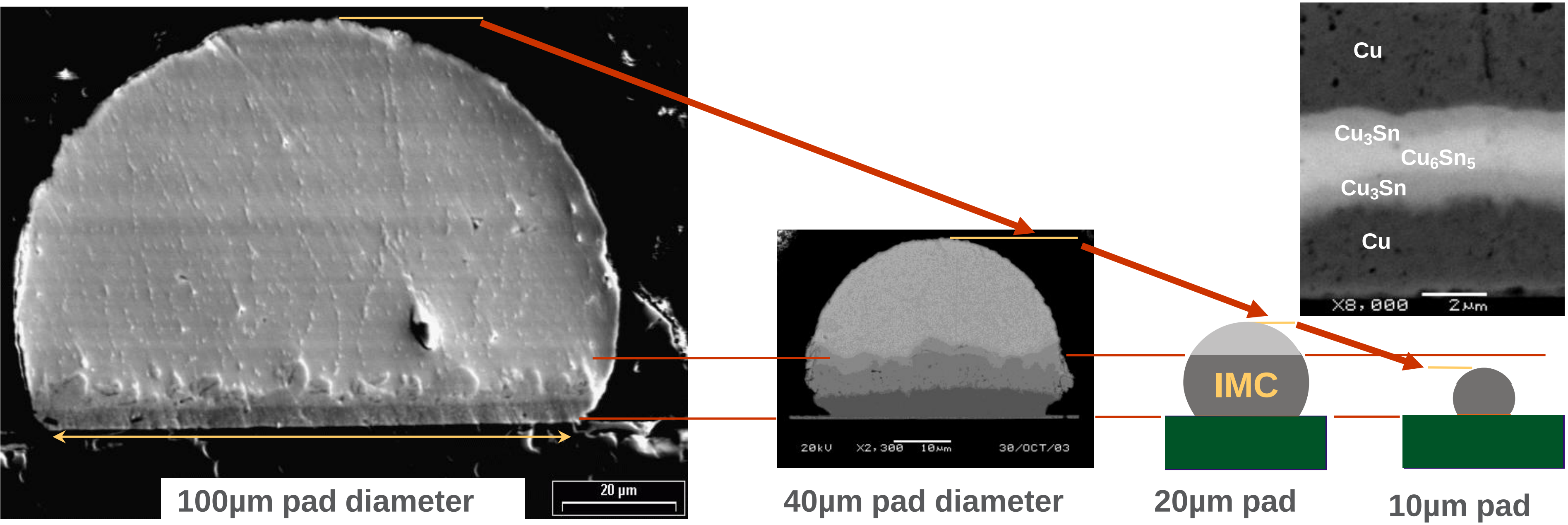

In


SnCu

Φ 25µm bump, 40/15µm pitch/spacing

HYBRID BACKSIDE ILLUMINATED IMAGERS: HIGH DENSITY BUMPING

- Flip-chip interconnect scaling:
  - Intermetallics formed by UBM solder interaction
  - Very small pitch: only intermetallic compounds
- Intermetallic bonding:
  - Advantage: have a higher melting point (and allow multiple layer stacking)
  - Disadvantage: multiple intermetallic compounds with variable reliability



100µm pad diameter
150-200µm bump pitch

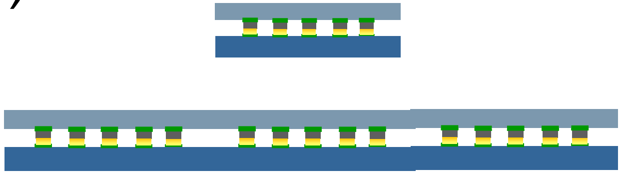
40µm pad diameter
60µm bump pitch

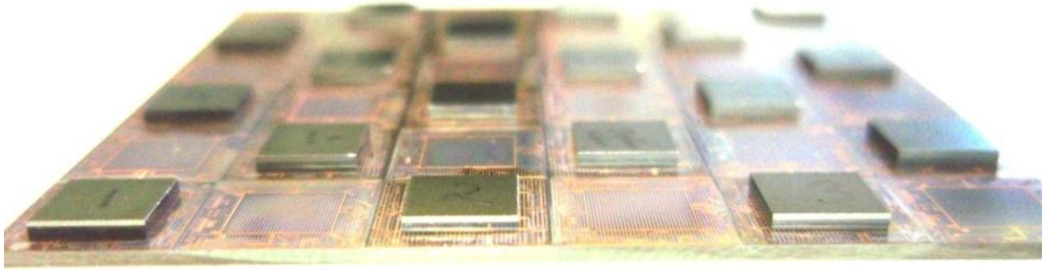
20µm pad
40µm pitch

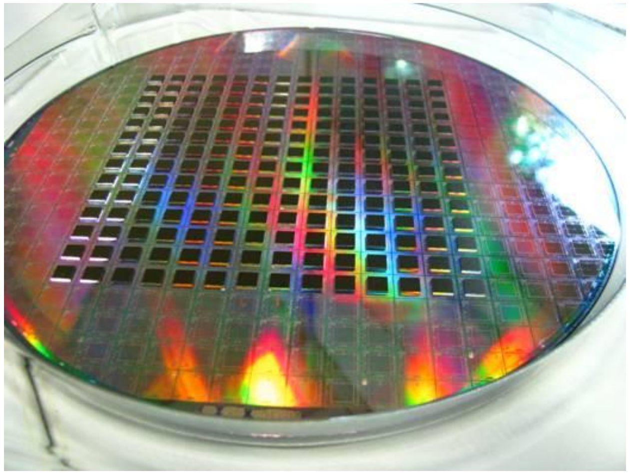
10µm pad
20µm pitch

HYBRID BACKSIDE ILLUMINATED IMAGERS: HIGH DENSITY BUMPING

- Bonding:
  - Thermo-compression (high T and force)
  - Different options:
    - Flip-chip: D2D, D2W
    - Wafer bonding: W2W
    - Collective bonding: 1) populate D2W 2) W2W bonding + anneal
  - Specialty: bonding of thin dies/wafers (on carrier)

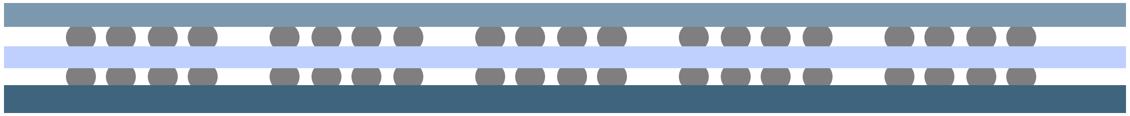




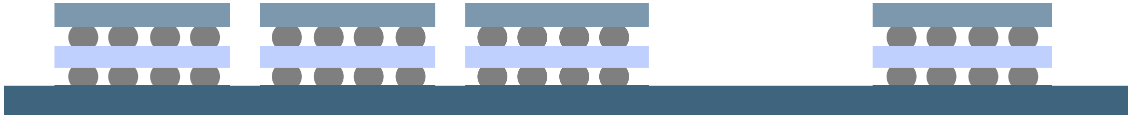


HYBRID BACKSIDE ILLUMINATED IMAGERS: HIGH DENSITY BUMPING

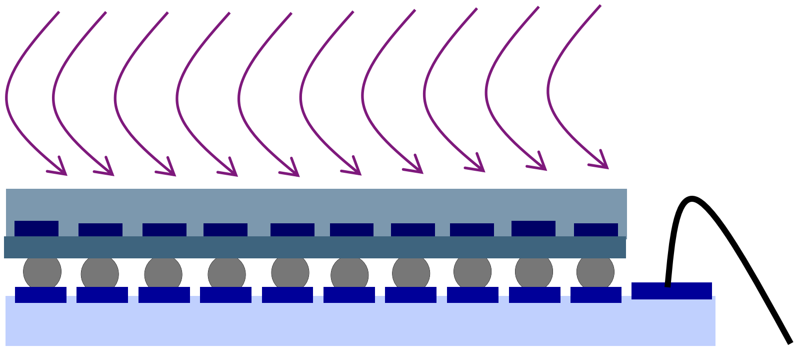
- W2W:
  - Advantages:
    - Technological ease: top layer can be thinned (and post-processed) after bonding to 2nd layer
    - Low cost
  - Disadvantage:
    - Equal chip size
    - Localization/processing of final outputs (unless using TSVs)
    - Compound yield may be low
  - Starts to be commercially available: MIT/Lincoln (SOI based), Tezzaron (but limited to 1 techno node)



- D2W:
  - Advantages:
    - Higher compound yield through Know Good Die (if testable !)
    - Different die sizes
    - Dies from different source wafers(i.e. different technologies) and from wafer sizes
  - Disadvantages:
    - More difficult process (hence higher cost): populate 'reconstructed' wafers (= serial process), maximal use of parallel processes (e.g. collective bonding)
  - Not yet commercially available: IMEC CMORE offering for small volumes

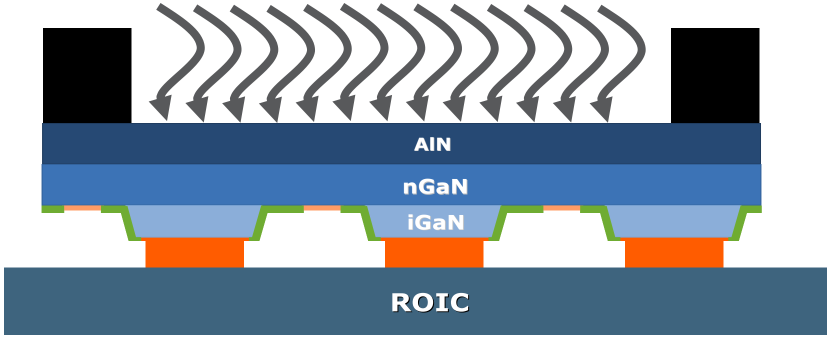


HYBRID BACKSIDE ILLUMINATED IMAGERS: HYBRID IMAGERS

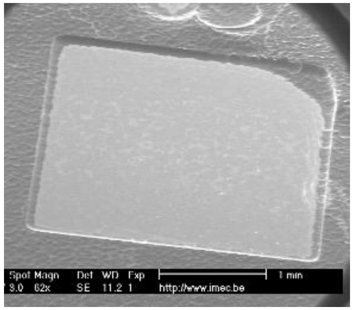


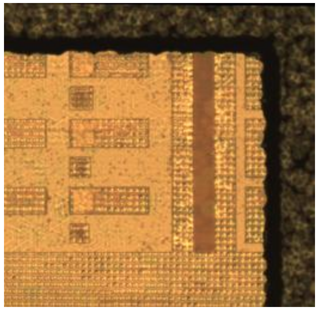
- Concept:
  - Face to face bonding using microbumps
  - 1 microbump per pixel
  - Top layer:
    - (typ.) Passive photodiodes
    - Choice of materials: Si (ev. high res), InGaAs, CdTe, (Al)GaN, ... for specific wavelength range detection (X-ray, UV, visible, IR, ...)
  - Bottom layer:
    - CMOS read-out circuit (ROIC)
- Advantage:
  - Different wafer material and/or technology top vs. bottom allows separate optimization
- Disadvantage:
  - Pixel pitch limited to bump pitch

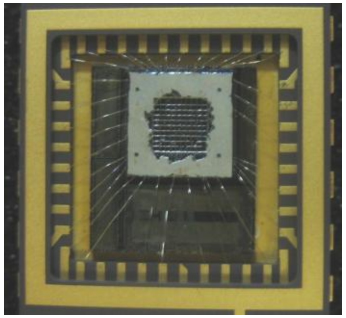
HETEROGENEOUS HYBRID IMAGERS:
(E)UV DETECTION USING ALGAN SCHOTTKY DIODES

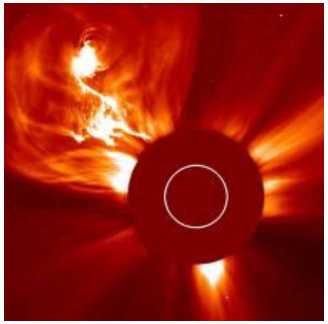


- Concept:
  - AlGaN growth on Si
  - Photodiode process
  - Flip-chip integration on ROIC
  - Backside etch of Si
    - Till membrane of < 1 um (!)
- Advantages vs. Si photodiodes:
  - Visible blind:
    - Due to large bandgap
    - Interest for e.g. sun observation
  - UV radiation tolerant
- Demonstration of 256x256 10 um pitch imager





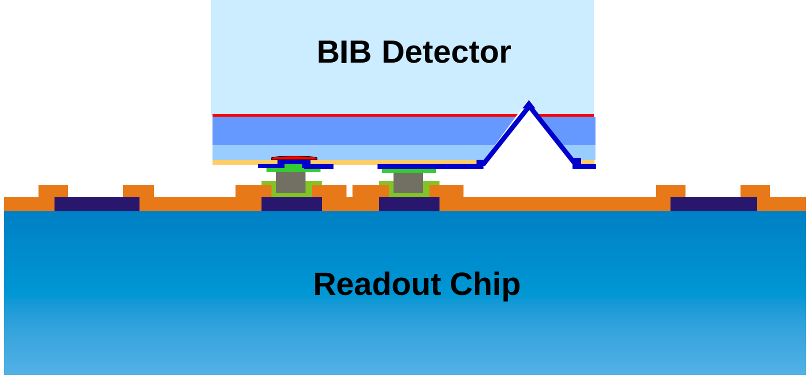


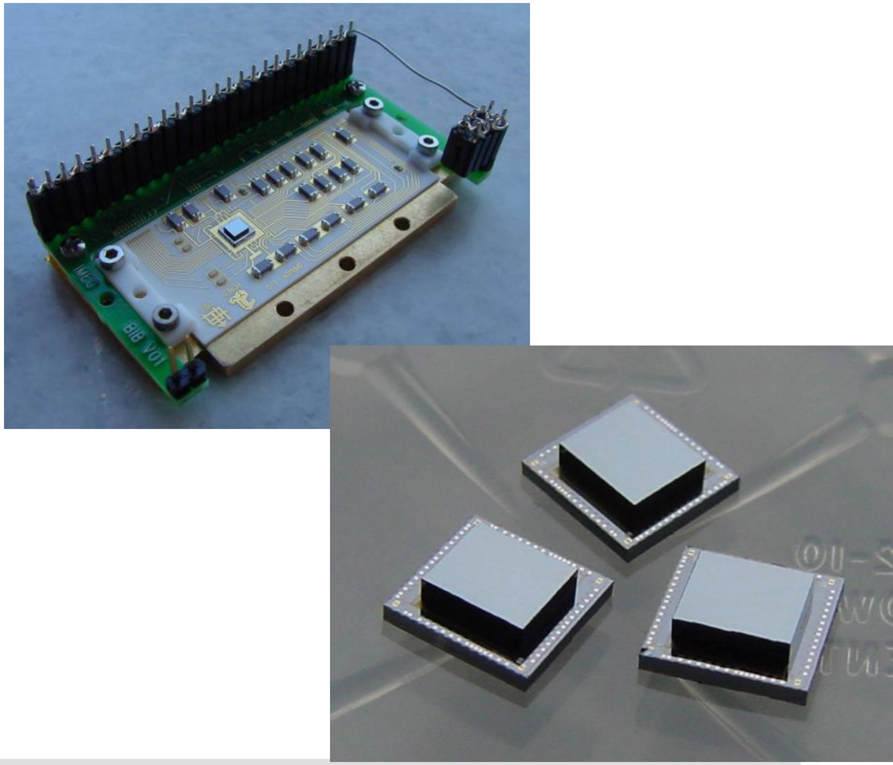


HETEROGENEOUS HYBRID IMAGERS:

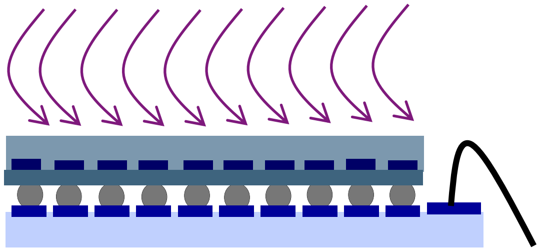
FAR IR DETECTION USING CRYOGENIC BIB DETECTORS

- Far IR detection (6-18 um)
- Concept:
  - Si:As Blocked Impurity Band (BIB) detector array operating at 4 Kelvin
  - Backside illuminated through high resistivity Si
  - Dedicated epi stack growth on Si
  - Contact process for buried contact and individual pixel
  - Flip-chip integration on cryogenic ROIC
  - In microbumps (for ultra-low temperature)
- Demonstration of bilinear array: 2x 88 pixels @ 30 um pitch
- Application: DARWIN mission:
  - Exoplanet atmosphere analysis

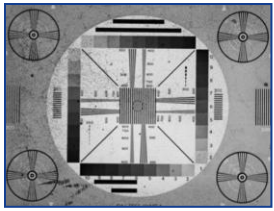




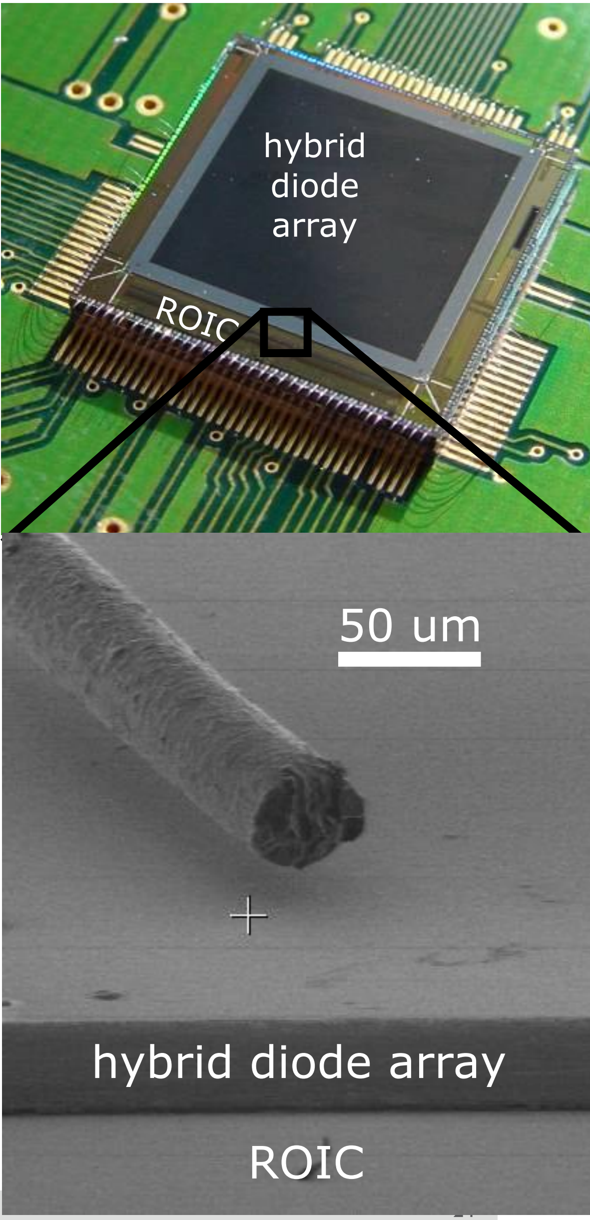
SI HYBRID IMAGERS FOR VISIBLE DETECTION: 'HYBRID APS'

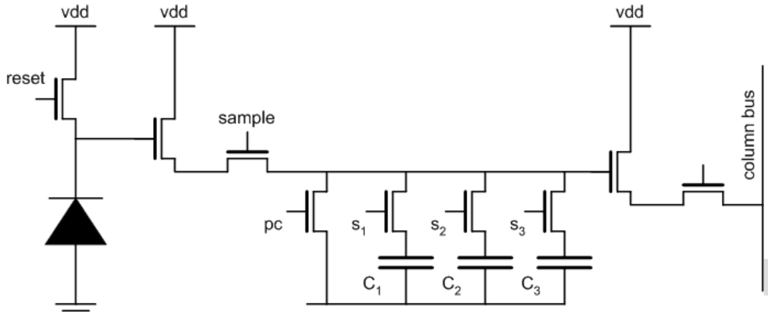


- Specifications:
  - 22.5 um pitch
  - Stitched design: 512x512, 1024x1024
  - **QE> 80% from 400 – 850 nm**
  - Thick epi: final thickness ~ 35 um

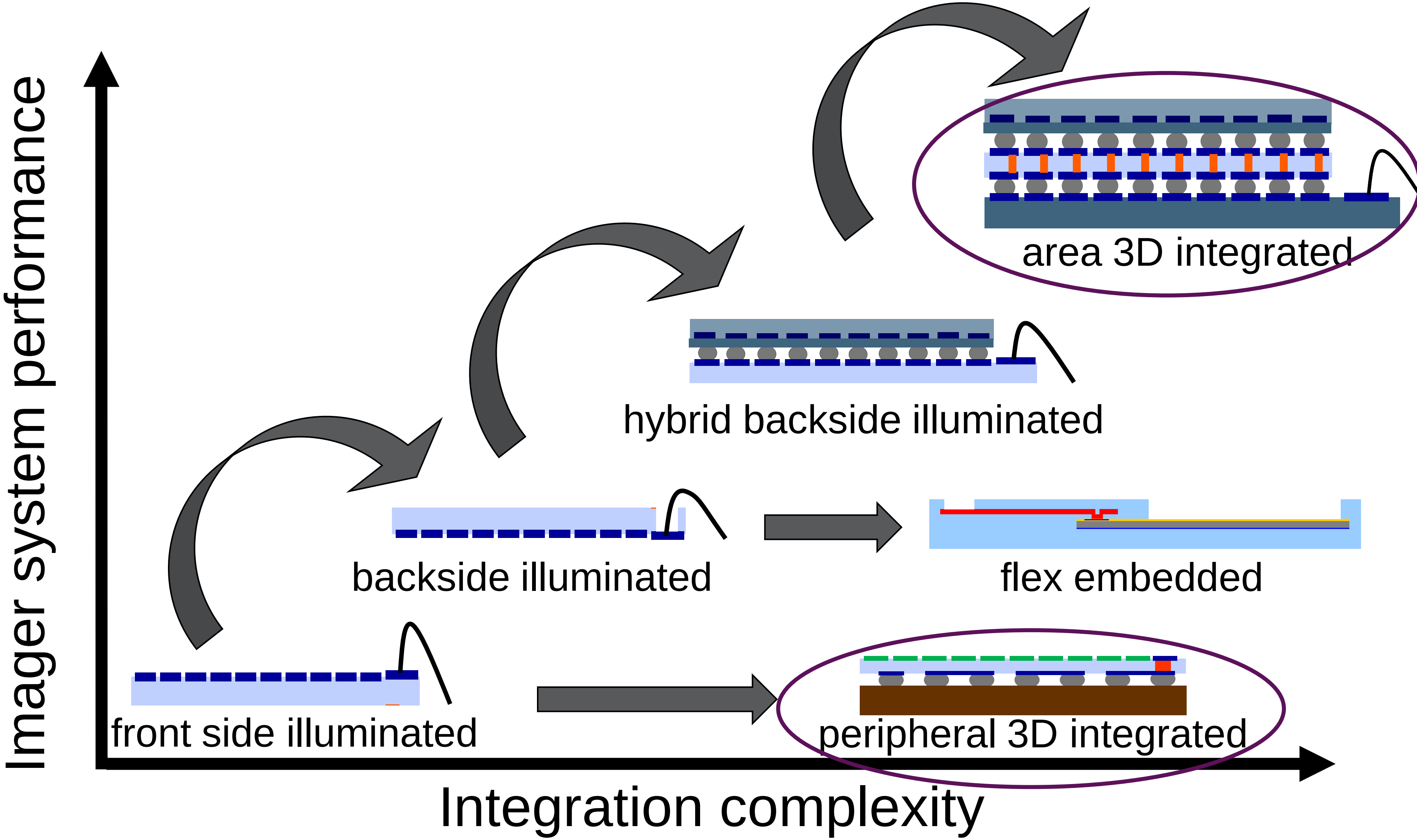


- ROIC designed by FillFactory/Cypress, fabricated in CMOS 0.35um foundry process:
  - **Snapshot**: synchronous pipelined shutter using 3 analog storage capacitors
  - On-chip Correlated Double Sampling (CDS)



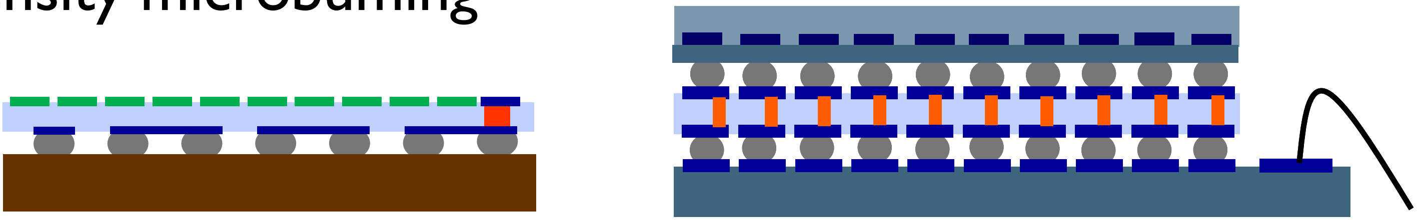


OUTLINE


Imager system performance
area 3D integrated
hybrid backside illuminated
backside illuminated
flex embedded
front side illuminated
peripheral 3D integrated
Integration complexity

3D INTEGRATED IMAGER TECHNOLOGY: INTRODUCTION

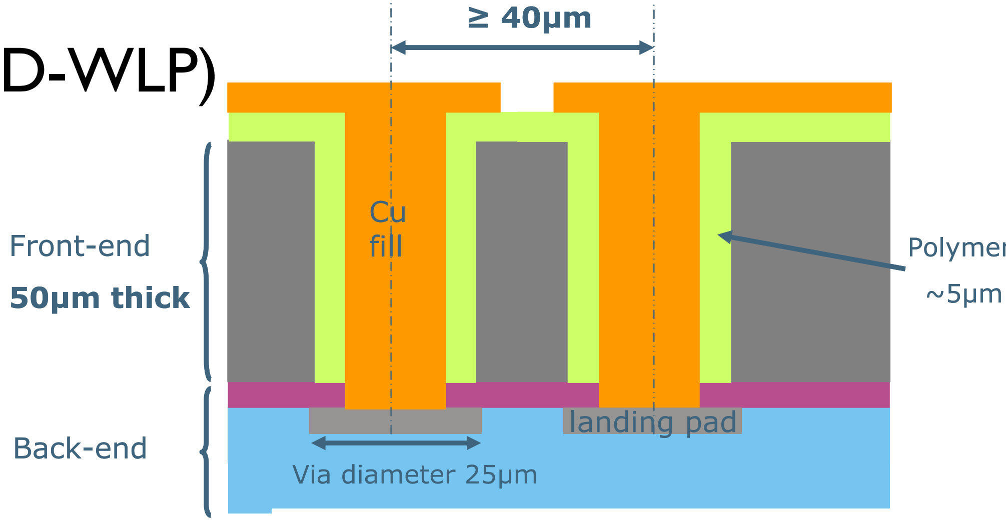
- = create vertical interconnect using combination of
  - Through-Si vias (TSVs)
  - High density microbuming

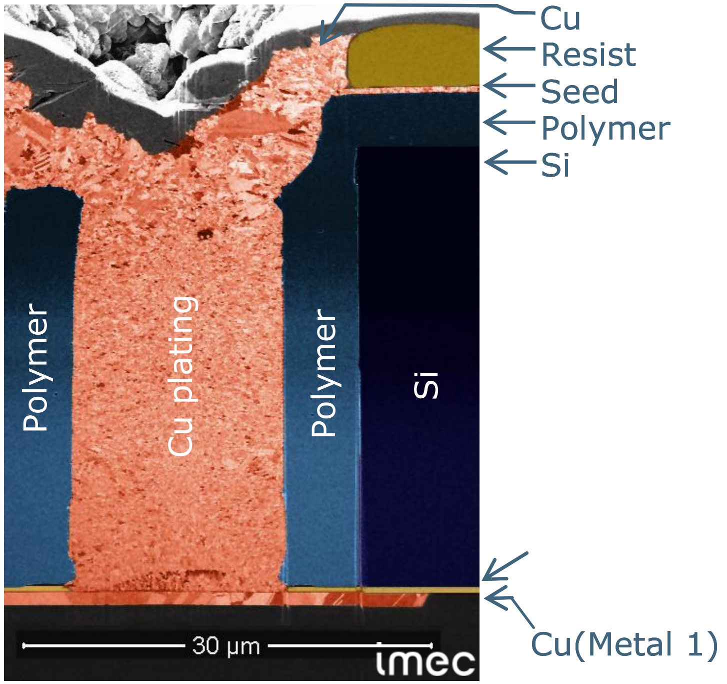


- Process sequence:
  1) Process TSVs and UBM/microbumps – on wafer level
  2) Assembly – D2D/D2W/W2W
- 2 options for TSV process:
  - After finishing CMOS processing = post-processing
  - During CMOS process

3D INTEGRATED IMAGER TECHNOLOGY:
3D-WAFER LEVEL PACKAGING

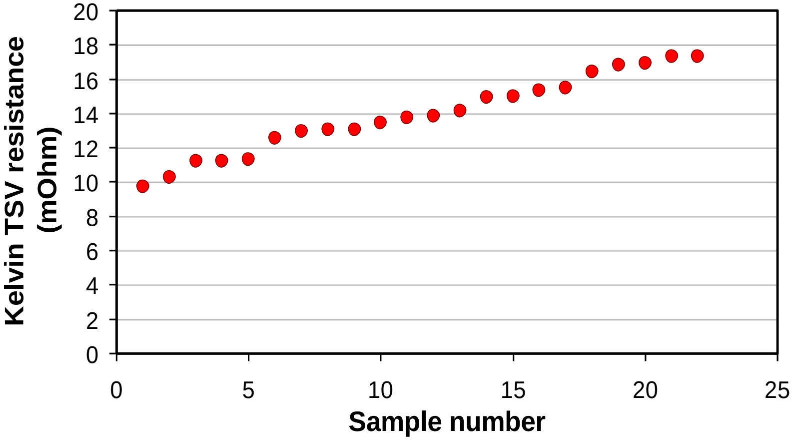
- 3D- Wafer Level packaging (3D-WLP) = post-processed TSVs
- Approach =
  - 1) Thinning
  - 2) TSV processing from the back
- Dimensions:
  - Minimal pitch = 40 um
  - Via diameter ~ 25 um
  - Si thickness ~ 50 um
- Via resistance < 20mΩ
- Low Capacitance: ~ 20 fF
- Design considerations:
  - Landing pad to be designed at lowest metal
  - Area consumption by TSV

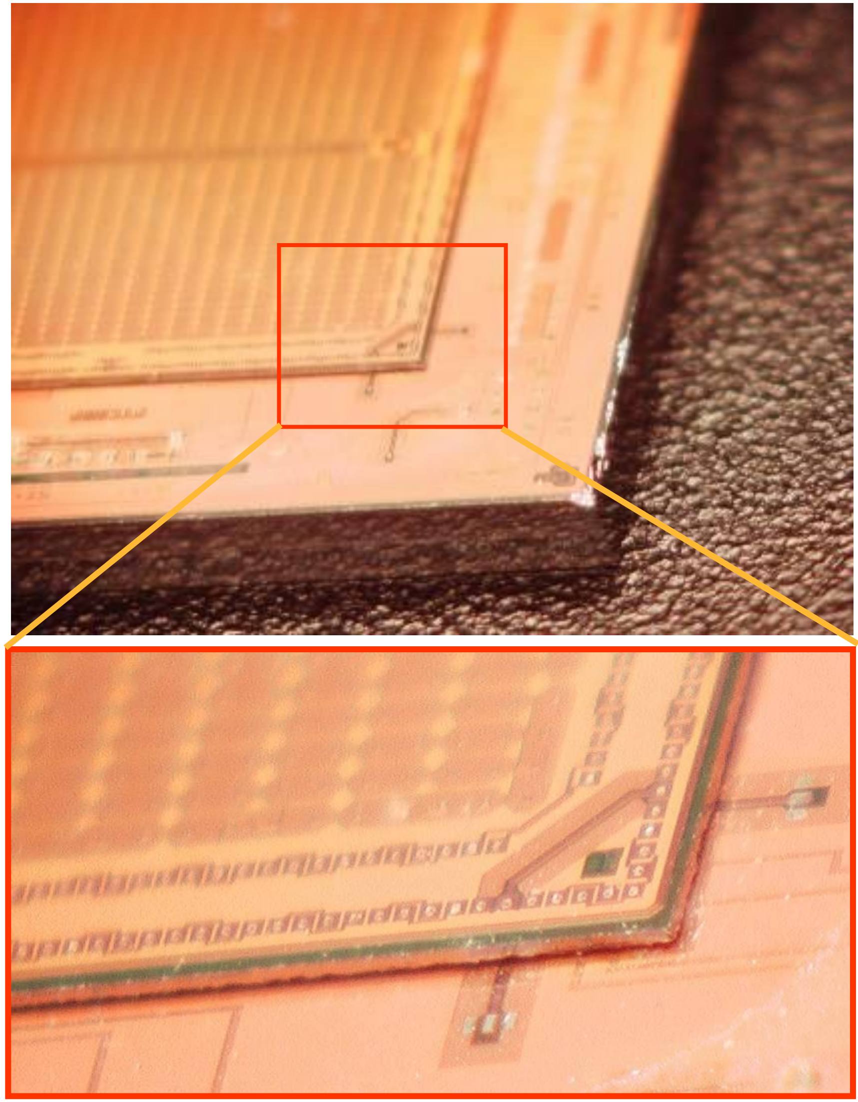




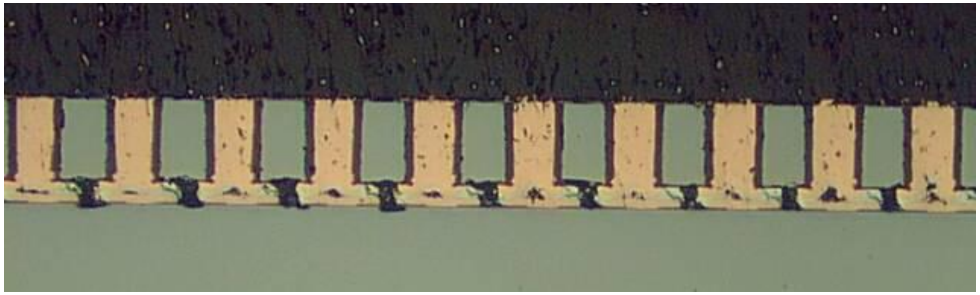
3D INTEGRATED IMAGER TECHNOLOGY:
3D-WAFER LEVEL PACKAGING

- Daisy chain demonstrator:
  - Electrical characterization



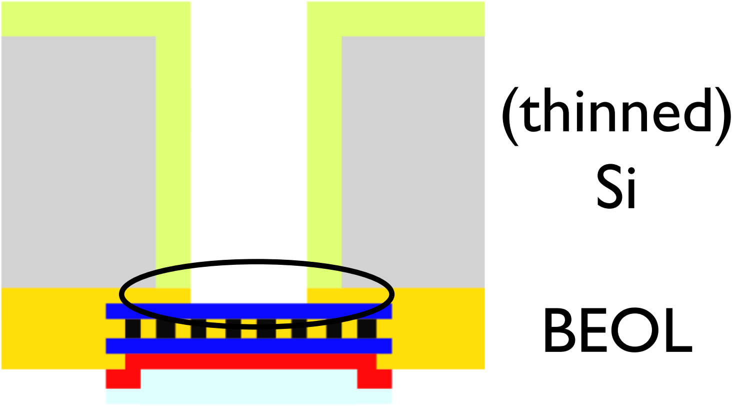


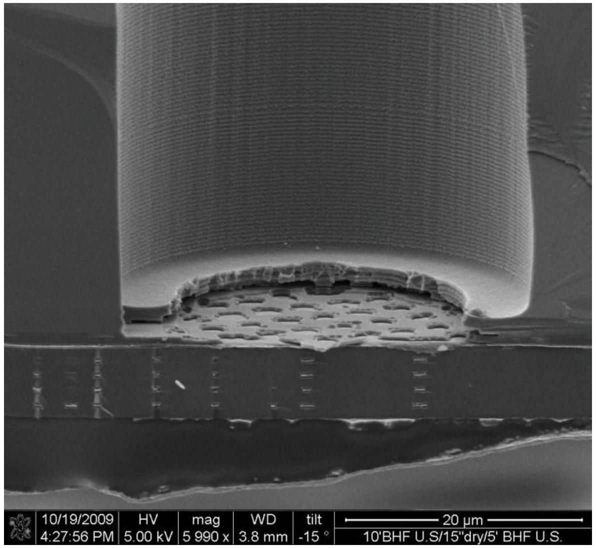
  - Reliability:
    - OK up to 1000 cycles - 40C/150C



3D INTEGRATED IMAGER TECHNOLOGY:
DESIGN FOR 3D STACKING

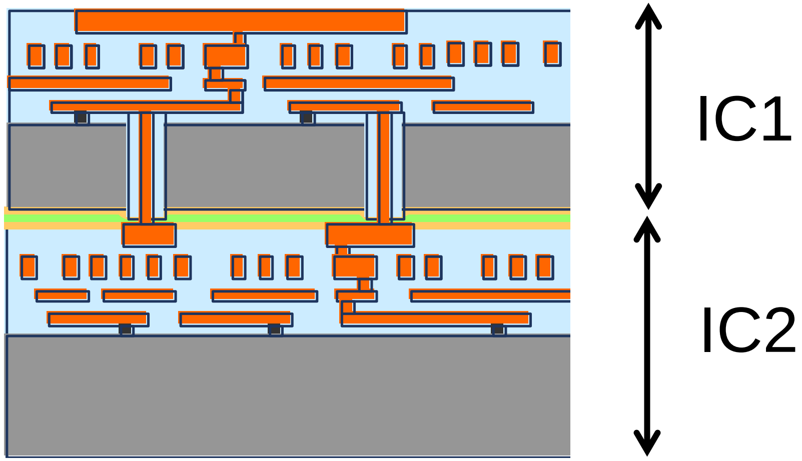
- Critical issue:
  - Etching (from the backside) of dielectric between lowest metal and Si
  - Presence of (difficult to etch) dummy features in CMOS technology (!)
- Solution:
  - Design for 3D stacking required
  - Dedicated design rule available (patented)

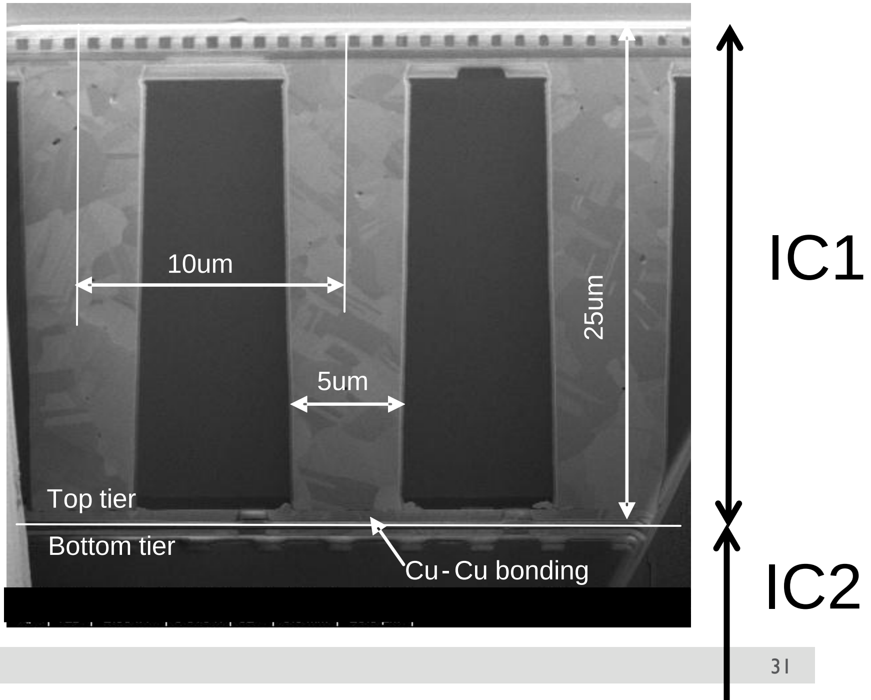




3D INTEGRATED IMAGER TECHNOLOGY: 3D STACKED IC (3D-SIC)

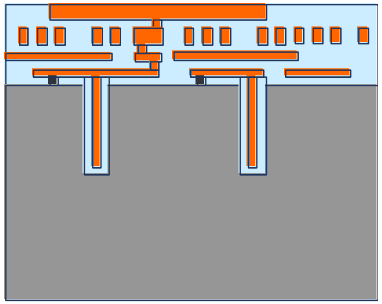
- 3D- Wafer level packaging = process TSVs as a part of the CMOS process:
  - At the level of the 1st metallization in the BEOL
  - Advantage: use of area above TSV
- Approach =
  - 1) CMOS process (incl. TSV)
  - 2) Thinning, TSV exposure, bonding
- Dimensions:
  - Minimal pitch = 10 um
  - Via diameter ~ 3-5 um
  - Si thickness ~ 15 um
- Via resistance ~ 20mΩ
- Via Capacitance: 40 fF (depletion)
- Design considerations:
  - Area consumption by TSV

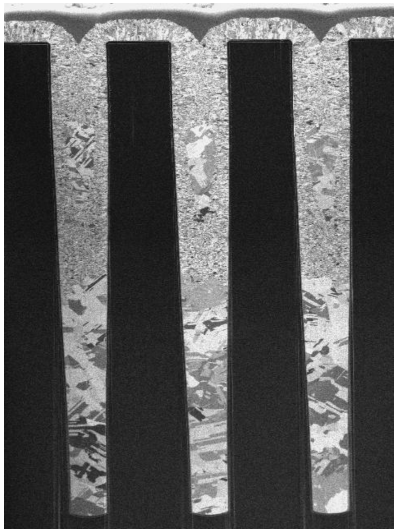




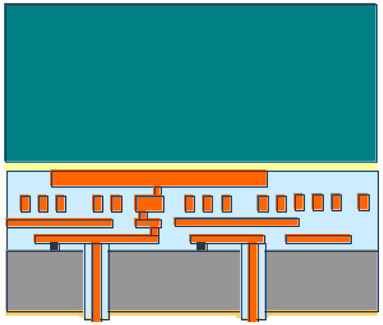
3D INTEGRATED IMAGER TECHNOLOGY: 3D STACKED IC (3D-SIC) PROCESS FLOW

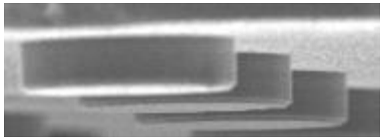
Via processing

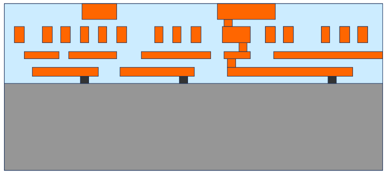




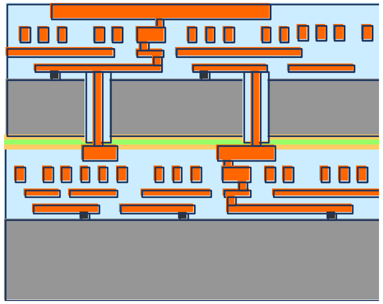
Extreme thinning
(on carrier)

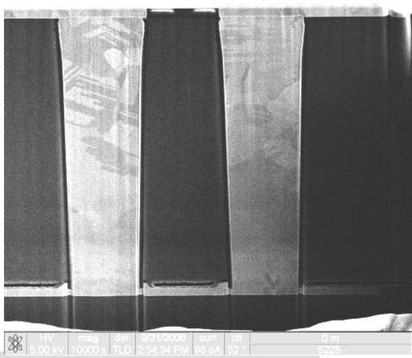






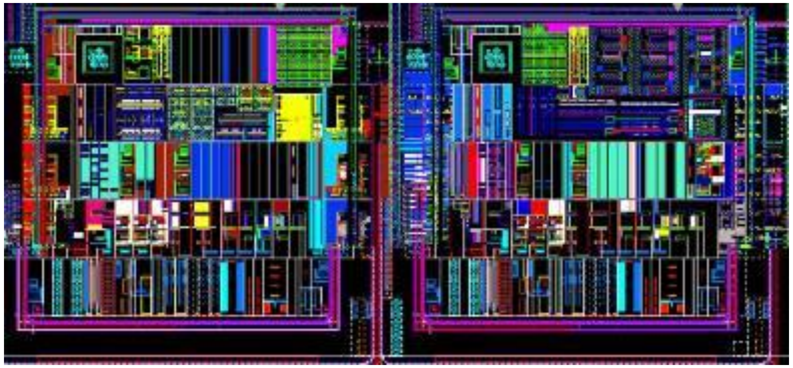
Mixed polymer and Cu-Cu
thermocompression bonding

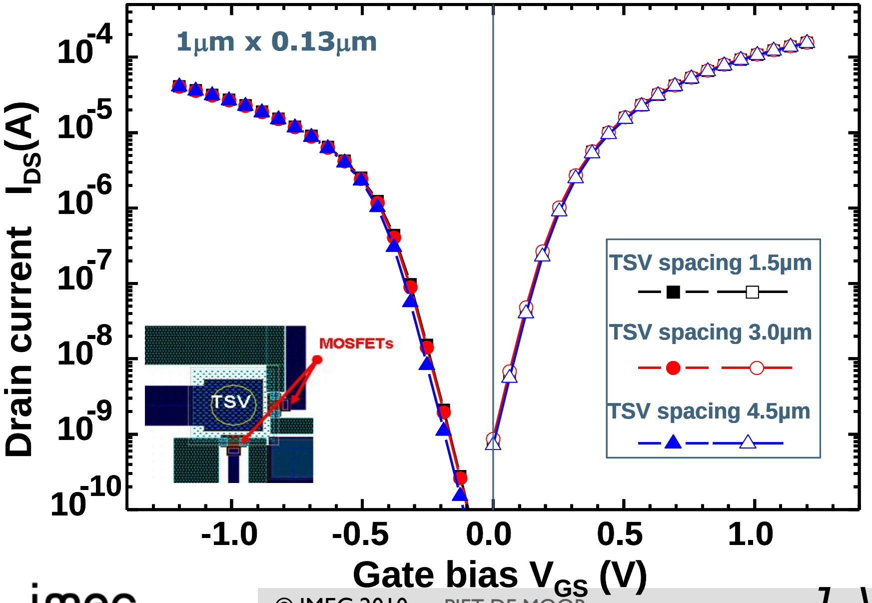


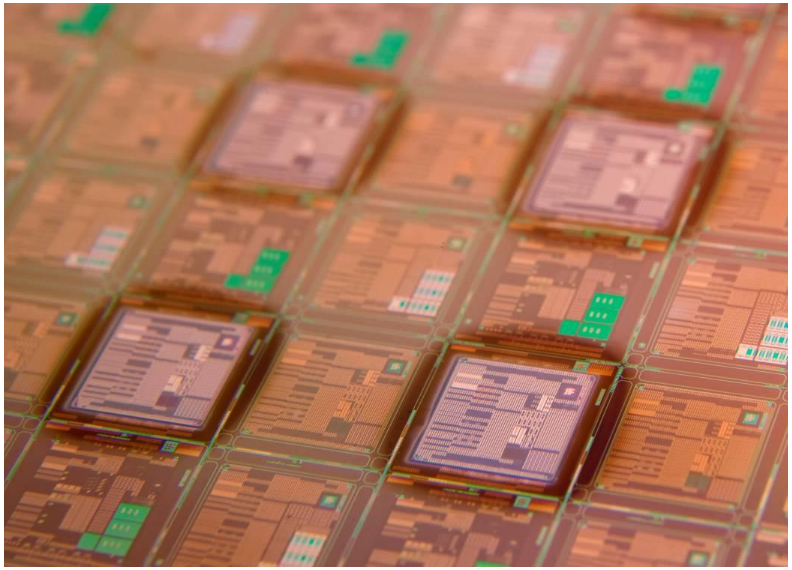


3D INTEGRATED IMAGER TECHNOLOGY:
3D INTEGRATION: 3D-SIC DEMONSTRATORS

- 3D Circuit Test Chip:
  - IMEC 130 nm CMOS 2 metal layers platform technology
  - Results:
    - I-V characteristics not affected by TSV for spacing down to 1.5 um
    - 3D Ring oscillator (100 TSVs) operational

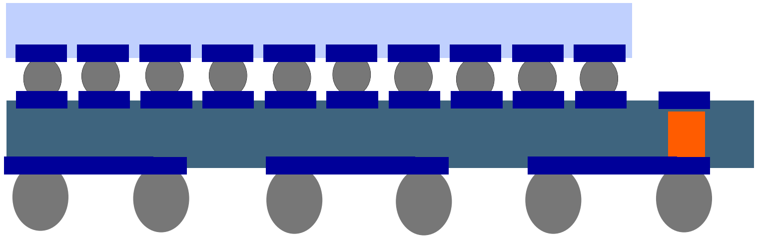




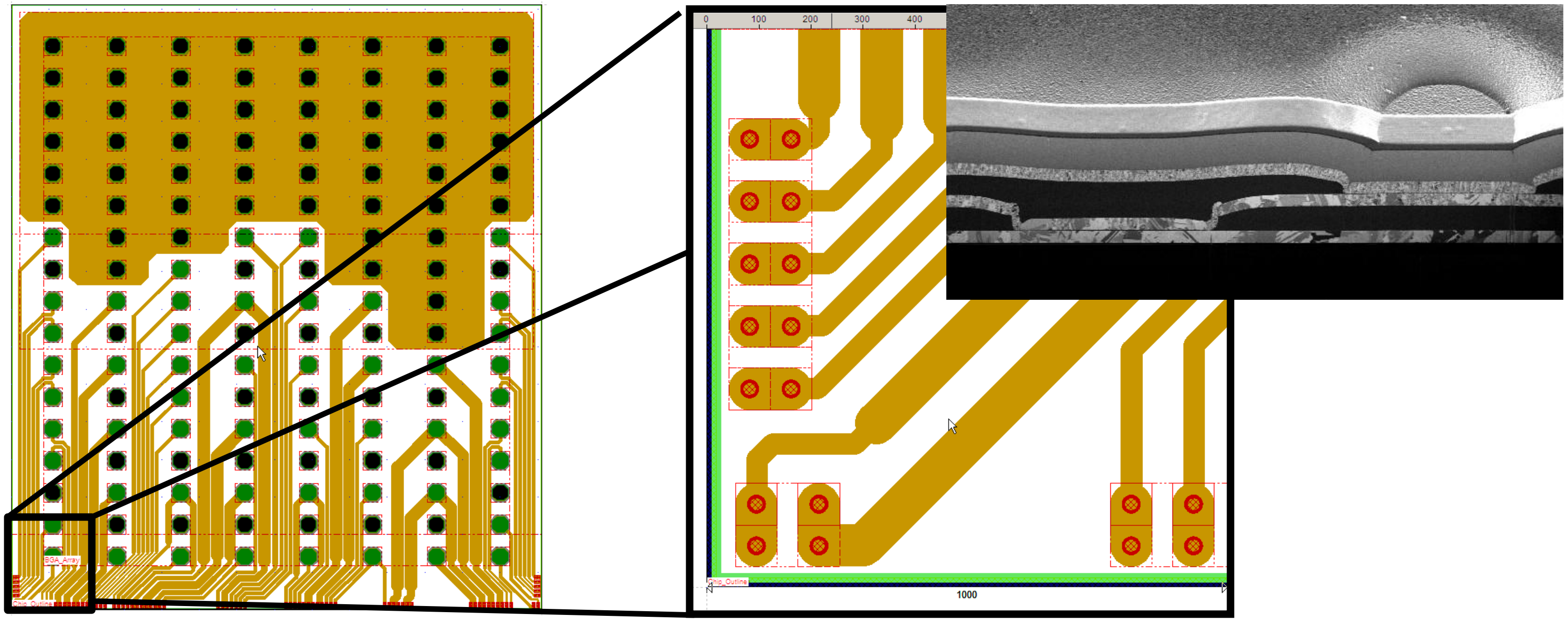


J. Van Olmen et al., IEDM 2008

3D INTEGRATED IMAGER TECHNOLOGY: REDISTRIBUTION LAYER

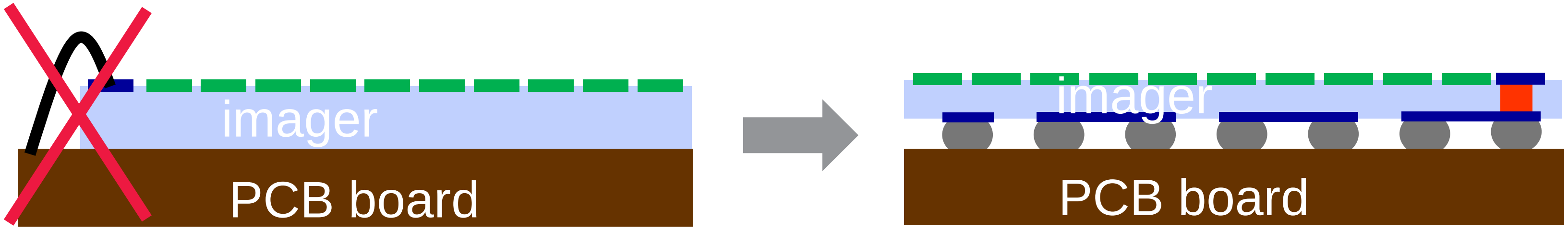


- Redistribution layer options:
  - Part of CMOS
  - At backside of (e.g.) TSV wafer
    - using e.g. Cu/dielectric



PERIPHERAL 3D INTEGRATED IMAGERS

- Advanced packaging technology at bond pad level:
  - From traditional lateral wire bonding to TSV per bond pad + bump ball bonding
  - = 3D integration at package level using Through Si Vias (TSVs)

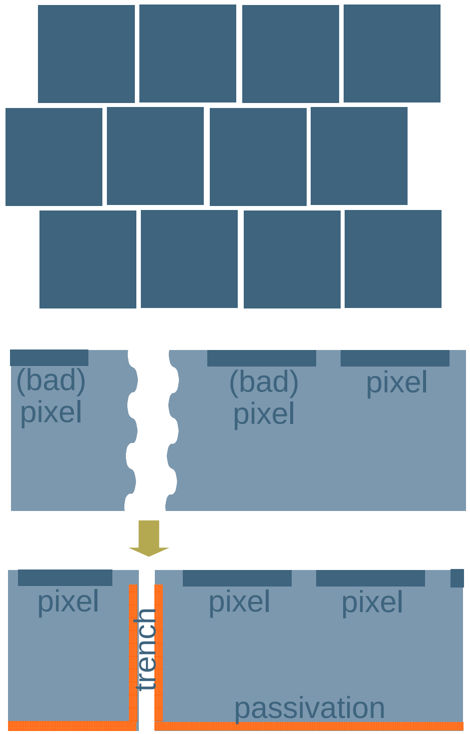


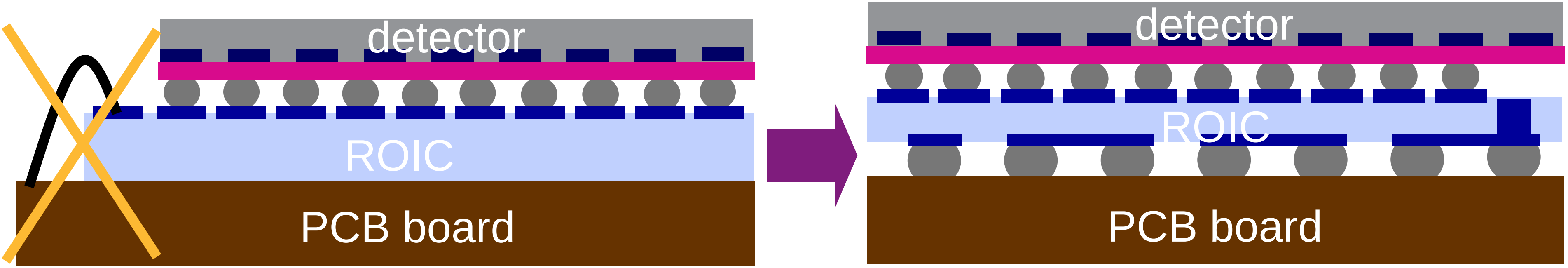
- Advantages:
  - Smaller footprint
  - Reduced capacitance → faster/low power interconnect
  - Buttability with mimimal area loss
- Applications:
  - Consumer imagers
  - Large area tiled imagers with minimal dead area
  - Endoscopes

PERIPHERAL 3D INTEGRATED IMAGERS:

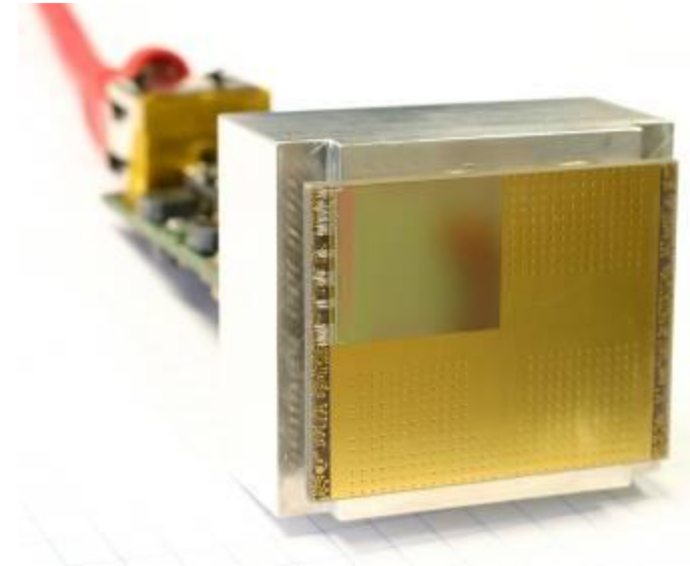
TILED EDGELESS IMAGERS FOR LARGE AREA DETECTION

- Large area imagers:
  - Stitching of large area imagers -> yield becomes critical
- Solution:
  - 4-side butting/tiling using 3D integration for vertical interconnections
  - Edgeless imagers: advanced singulation close to active pixels:
    - Dicing by grinding
    - Side wall passivation

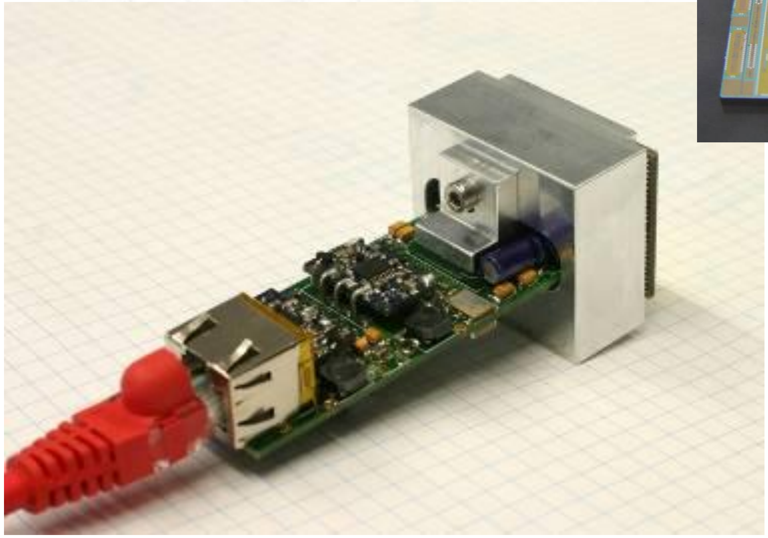


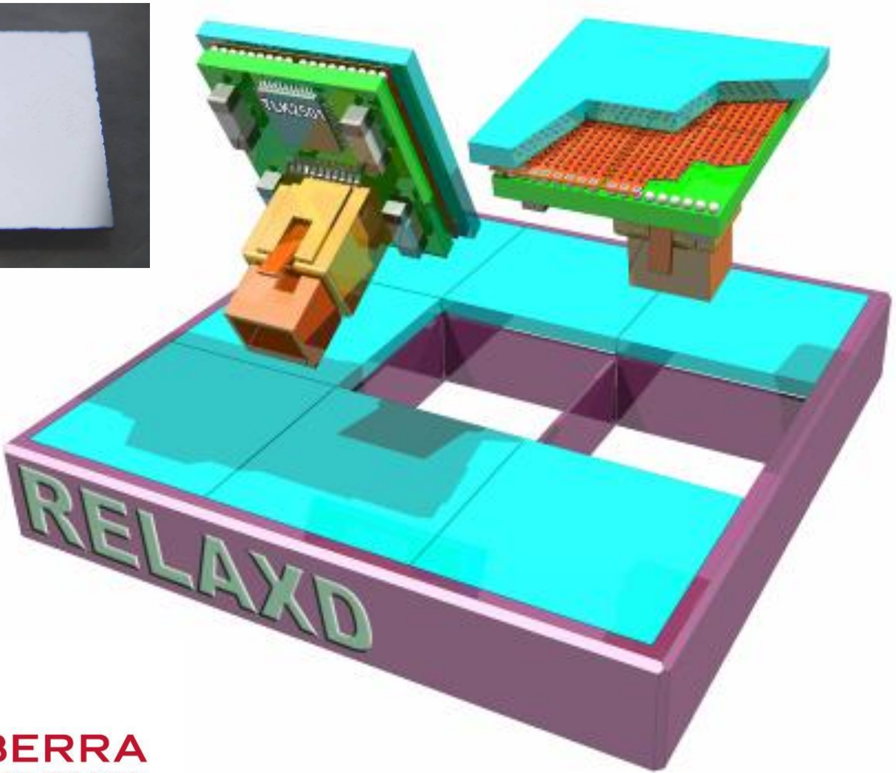


TILABLE X-RAY IMAGERS USING IMEC 3D INTEGRATION: RELAXD



- X-ray detector hybridised on Medipix ROIC with post-processed TSVs
- status: close to demonstrator

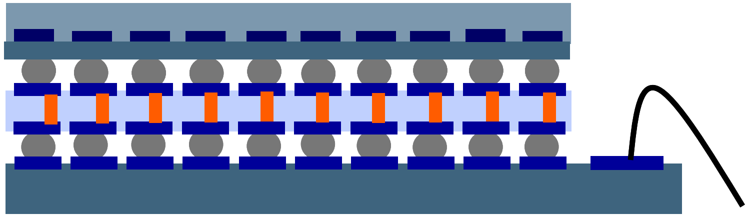




PANalytical NIKHEF

CANBERRA
AN AREVA COMPANY

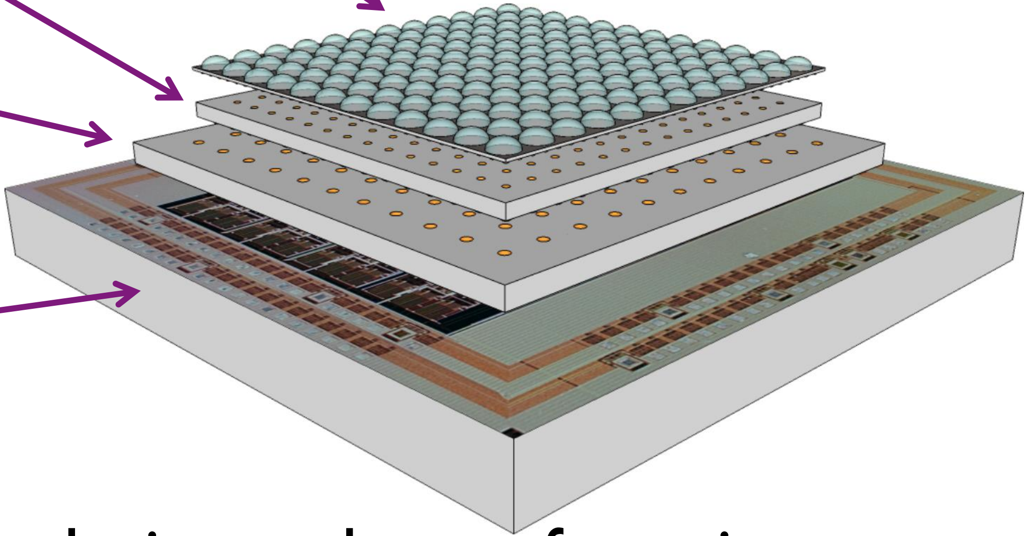
AREA 3D INTEGRATED IMAGERS



- Concept:
  - Stacking of multiple (>2) layers: detection layer + ROIC layers
    - Example: passive photodetector layer + analog ROIC + digital image processor
  - Using high density bumping + area redistributed TSVs
- Advantages:
  - General: optimization of (CMOS) technology for different layers
  - Imager system:
    - Vertical parallel readout chain allows high speed
    - Triple (n-fold) area per pixel allows complex electronics per pixel
    - Low capacitance interconnect to digital image processor allows high speed and low power
- Challenge: system architecture:
  - Optimal split in different layers of functionality and technology

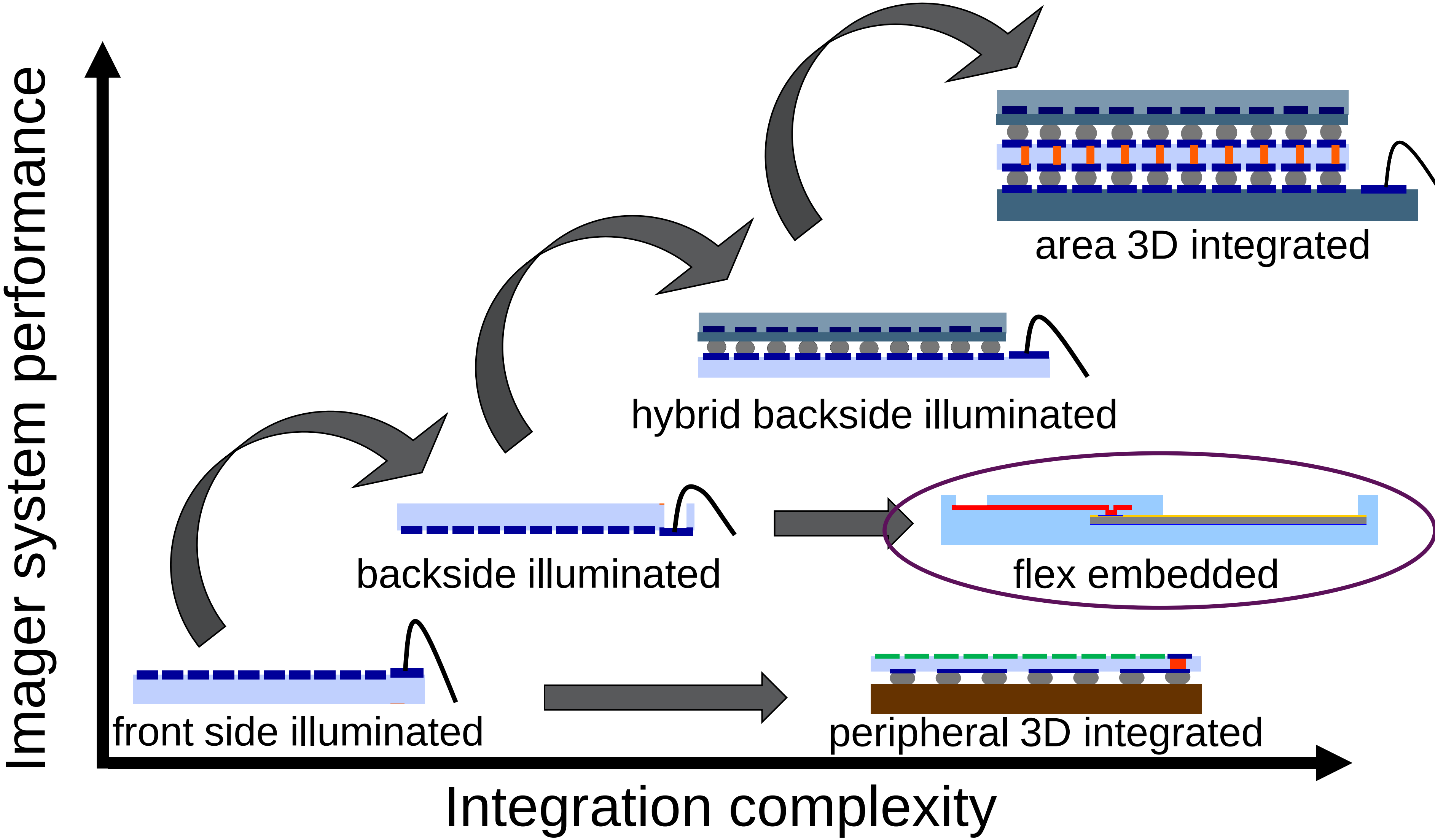
AREA 3D INTEGRATED IMAGERS

- Status: system architecture study of an **imaging system on a chip-stack**
  - Integration of micro-optics layer:
    - Ultra wide field of view
    - Filters for hyperspectral imaging
  - Shared pixels = multiple pixels per bump
  - Smart analog/digital read-out:
    - Ultra high dynamic range
    - ADC per group of pixels
    - Variable resolution (active binning)
  - Smart digital processing:
    - 2D distributed group of processors
    - Face recognition



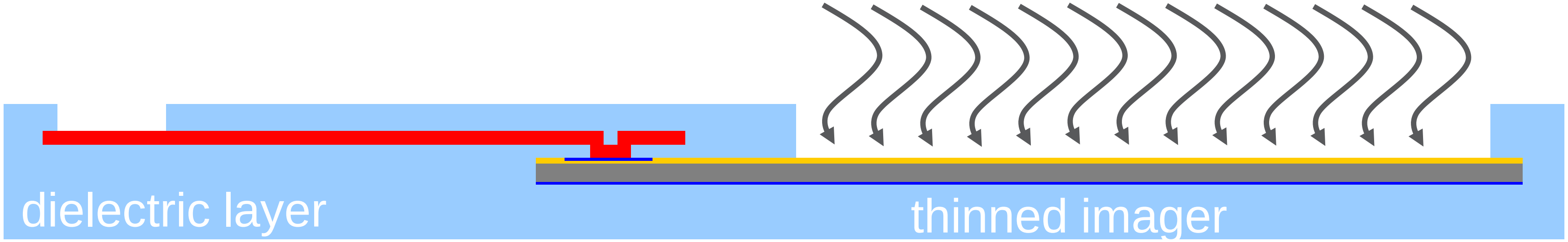
- Next step: demonstrator design and manufacturing

OUTLINE

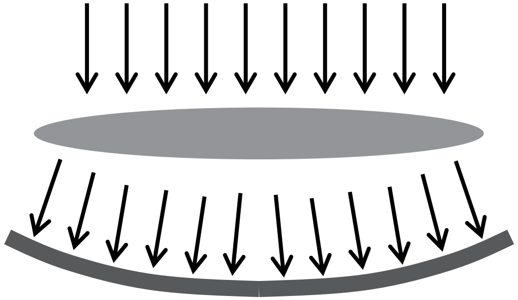

Imager system performance
area 3D integrated
hybrid backside illuminated
backside illuminated
flex embedded
front side illuminated
peripheral 3D integrated
Integration complexity

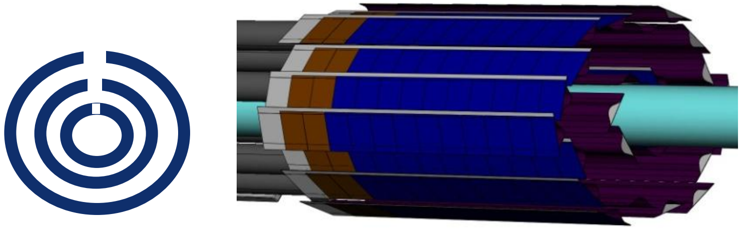
ADVANCED INTEGRATION: FLEX EMBEDDED IMAGER

- Concept: embedding of a thinned imager in a flexible foil

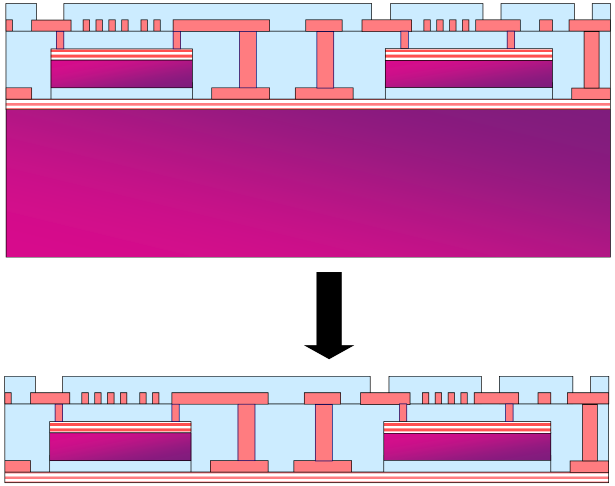


- Applications:
  - Non planar (bended) focal plane camera:
    - Low cost & optimized lens design
  - On/in the body radiation monitoring for cancer therapy
  - Tracking detectors for high energy particles:
    - Low scattering (very thin)
    - Bendable



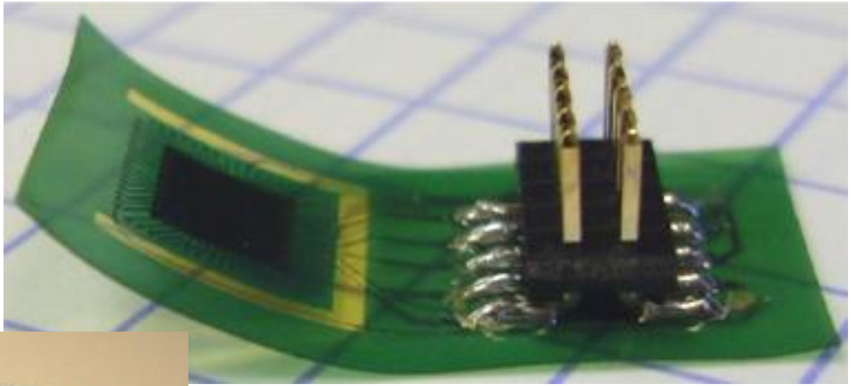


ADVANCED INTEGRATION: FLEX EMBEDDED IMAGER



- Technology:
  - Extreme wafer thinning (20 um)
  - Embedding on flex
- Example of related IMEC techno:
  - Functional microcontroller in flex substrate
- Embedding of tracking imager ongoing

IPHC
Institut Pluridisciplinaire
Hubert Curien
Strasbourg



CONCLUSIONS

- Advanced 3D integration technology enables smart imagers with high performance
- The best integration scheme is application dependent
- imec has capabilities in:
  - Backside thinning and passivation
  - High density bumps
  - Through Si vias
  - Advanced assembly
- imec can offer specialty product development on demand up to small volume production (CMORE)

ACKNOWLEDGEMENTS

- Program managers:
  - Eric Beyne: Advanced Packaging
  - Bart Swinnen: 3D integration
- Members of different departmens/teams involved:
  - Interconnect & packaging department: Bart Swinnen
  - Packaging Microsystems Hybrid Technology group:
    - Philippe Soussan, Deniz Sabuncuoglu, Francois Iker, Paresh Limaye
  - Heterogeneous Integrated Microsystem department: Chris Van Hoof
  - Heterogeneous Component Integration group:
    - Koen De Munck, Kiki Minoglou, Padmakumar Rao
- Funding by:
  - Industrial partners, equipment suppliers
  - European commission, Flemish Government, European Space Agency

ASPIRE
INVENT
ACHIEVE

imec