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New interconnect technologies

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Although CMOS technology has a proven track record in terms of performance, there are limitations of a single chip (and even more of a full system containing many chips) in terms of the traditionally lateral interconnects. The past years a lot of R&D was spent to develop 3D interconnect and integration technologies such as high density bump interconnects, through Si vias and advanced assembly. Implementation of these technologies in 3D stacked systems are expected to enable more preformant electronic systems. In this talk, an overview of the technology building blocks and their maturity status will be given, as well as a number of examples in imaging applications developed at imec.

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