Contribution ID: **170** Type: **Oral**

3D-IC MPW runs for HEP

Tuesday 21 September 2010 14:15 (45 minutes)

3D-IC integration world is a rapidly growing where several scientific communities and companies are addressing important R&D resources. Among them the HEP community, through the FermiLab action who made in the few last years a significant leapfrog offering some fabrication's runs.
The number of events and publications in this field is also growing significantly.

CMP is a non-profit / non-sponsored organization offering services, for IC manufacturing for prototyping and low volume production. Since 1981, the service is providing the support for design-kits distribution & support, CAD tools, wafer fabrication, and sawing / packaging.

CMP jointly with MOSIS (USA) and CMC (Canada) announced the intention to offer services on the 3D-IC process from Tezzaron based on a 130nm CMOS process.
Different developments achieved already and others are ongoing regarding especially the design flow supporting the users, and the choice of the 3D-IC process options.
Processes and design-flows are linked, since modifying one or several features in the 3D process will involve changes in the design flow then inducing new features and developments in the design-kits and CAD tools.

The selection of the 3D process has been fixed. The Design Platform (TDP) containing the (PDK) Process Design Kit and the cells libraries has been integrated in a unified environment.
The collaborative work between CMP, the HEP community and the partners MOSIS and CMC, resulted in a unique and unprecedented design environment.
Innovative tools and solutions inside this platform are making a much more productive environment.

New features in the design methodology 3D-IC were needed for both the full-custom design-flow and the automatic semi-custom flow. They involve the layout edition, and verification (3D DRC, 3D LVS), 3D automatic place and route, dummies filling strategy, etc ⋯
3D-IC integration needs new design paradigms making the difference with SiPs (system in package). The main difference would be the use of the 3rd dimension as a regular interconnection. That 3rd dimension represents TSVs (Through Silicon Via) or DBIs (Direct Bond Interface). They have to be used not only as connections through the IOs in the periphery of the tiers'chips or blocks, but connecting in a way that a blocks or chips are distributed across the tiers. CAD tools enabling optimized partitioning don't exist yet in the industry. The more the partitioning involves small blocks and small leaf-cells, the more the floor-planning will be efficiently optimized. The resulting system will not be easy to test as it will not be a simple stack of "Known Good Dies" as this is done for SiPs systems.
Real 3D-IC integration will then not be considered as a simple stack of dies like for SiPs.
This is like for buildings. They cannot be made by simply stacking individual houses.

Presenter: TORKI, Kholdoun (CMP)

Session Classification: PLENARY 2 - 3D MPW runs for HEP