SEU WORKING GROUP

GOALS
Define Level and Types of SEE Problems
Appropriate Mitigation
What's already done
needs Study
Provide Repository for Results

TWEPP 2010

Mitigation of Single Event Effects

SEE Domains

- ASIC Design → Today's topic
- FPGA Design → J. Christiansen announcement

Determine Mitigation requirements

Acceptable rates of

- Compromised of functional fidelity
- Loss of data integrity

What Level of mitigation is required?

Which ASIC Technology ?

Presentations / Conclusions

- Three presentations:
  - Federico Faccio (CERN)
  - Sandro Bonichi (CERN)
    - Work at CERN in 130nm
  - Moshine Menouni (CPPM)
    - FEI4 mitigation approach (some cells without mitigation to help calibrate effectiveness)
- Web Archive of work, meetings, issues to be made available to the community.

CERN-PH/ESE
F.Faccio, S.Bonacini

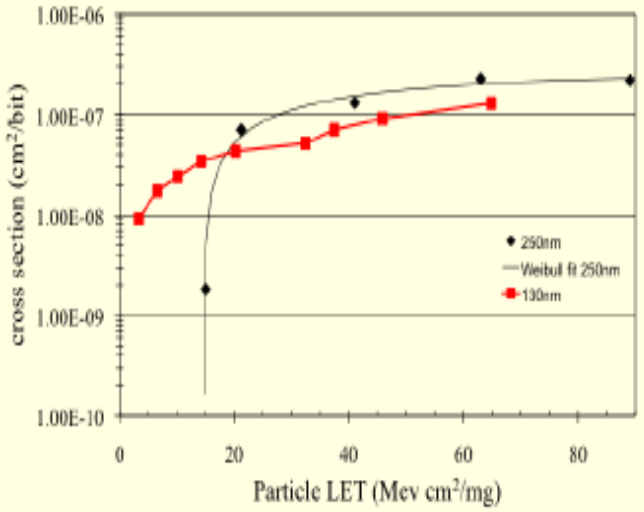
Available radiation data for "hardened" cells (proton tests)

- Wide range of "hardened" cells custom designed and tested (200MeV protons) by FNAL. Results presented by J.Hoff in 2006.
  - Some of them have cross-section 3 orders of magnitude below the one measured for a commercial cell
- DICE cells custom designed and tested in 2008 by the ATLAS Pixel detector collaboration
  - results presented by M.Menouni at TWEPP 08
  - 3 different layouts integrated
  - Tests done with the CERN 24 GeV/c proton beam
  - Cross-section varies with layout but mainly around $2\text{-}3\cdot10^{-18}$ cm^{2}bit^{-1}.
    - This is 10 times larger than what measured by FNAL on the same design in 2006
    - (but different layout and proton energy).

Type	Cross Section
LBL Dice	3.84e-17 cm^2/bit
RT Dice	5.86e-17 cm^2/bit
RT Seuss	1.03e-15 cm^2/bit
RT SR-ff	3.85e-14 cm^2/bit
RT normal	3.23e-14 cm^2/bit
TR Seuss	4.7e-15 cm^2/bit
TR SR-ff	8.91e-15 cm^2/bit
Hit	1.59e-15 cm^2/bit
Liu	2.69e-16 cm^2/bit
Dice	4.55e-15 cm^2/bit
Seuss	1.05e-14 cm^2/bit
SR-ff	5.02e-14 cm^2/bit
COMMERCIAL	4.86e-14 cm^2/bit
Normal	5.63e-14 cm^2/bit

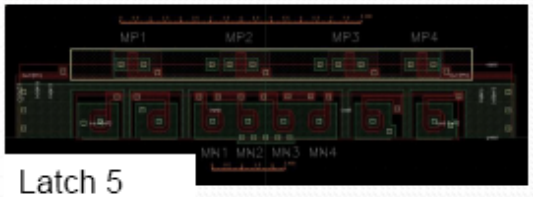
Comparison with 250nm FF

- Comparison with 0.25μm FF (using ELTs):
  - Cross-section of the commercial 130nm design orders of magnitude larger in LHC environment – the 0.25um design had a threshold close to the maximum LET possible from nuclear interaction in Si

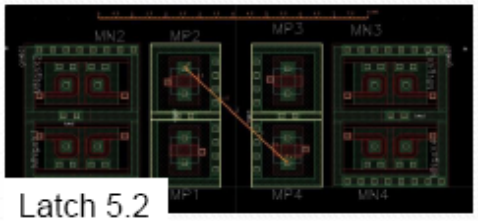


CPPM-CNRS (Moshine Menouni)

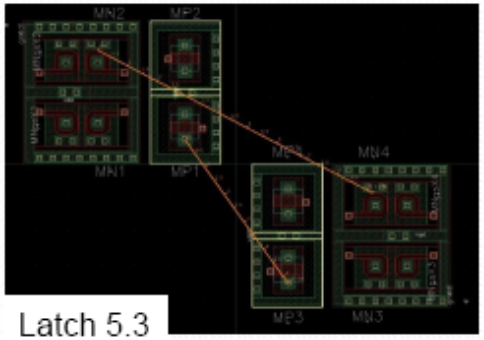
Layouts implemented in the chip SEU2



Latch 5

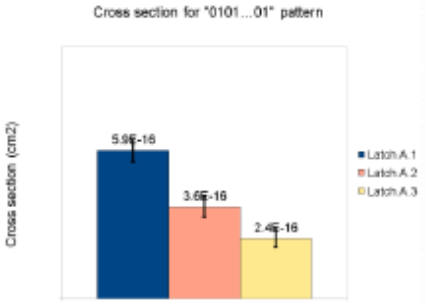


Latch 5.2



Latch 5.3

Latch type	area	Cross section cm²/bit		
		1->0	0->1	1->0 and 0->1 (*)
Latch 5	48 µm²	(1.5 0.1).10⁻¹⁶	(2.2 0.3).10⁻¹⁶	(5.9 0.5).10⁻¹⁶
Latch 5.2	48 µm²	(3.4 0.6).10⁻¹⁶	(4.2 0.4).10⁻¹⁶	(3.6 0.5).10⁻¹⁶
Latch 5.3	48 µm²	(3.0 0.6).10⁻¹⁶	(3.3 0.3)10⁻¹⁶	(2.4 0.5).10⁻¹⁶



Measurements made in 2008 for the chip SEU2

- Different layout versions were implemented in the SEU2 chip
  - Same schematic but different layout
- The latch 5.3 is 2.5 times tolerant to SEU than the latch 5
- This result shows the importance of separating sensitive nodes