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Design and characterization of an SEU-robust register in 130nm CMOS for application in HEP ASICs

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A new SEU-robust D-flip-flop register structure was designed in 130 nm CMOS for utilization in a rad-tolerant library. The register was tested in a heavy ion beam facility and showed a cross section lower than 1e-10 cm²/bit in the LET range (1.2 –62.0 MeVcm²/mg) representing an improvement of 1000 times over previously studied standard library cells. No errors were observed at LETs under 30 MeVcm²/mg.

Summary

The design of HEP experiments often requires the development of ASICs, which are robust to Single-Event Upsets (SEUs). This work focuses on the design of an SEU-robust register cell, compatible with the radiation environment present in the tracker sub-detectors of the experiments around the Large Hadron Collider (LHC).

Triple Modular Redundancy (TMR) is a typical solution to the vulnerability of flip-flops in digital logic, but has significant drawbacks because of the increased power consumption and area implications. These are problematic for the construction of future higher performance detectors with an increased number of channels where the power per channels should instead be reduced.

The solution proposed in this work is an SEU-robust cell which requires only a double redundancy of the circuitry with respect to a standard D-FF. Our solution is based on the DICE scheme which –as it is well known - is intrinsically SEU-hard to single-node particle hits. Additional layout techniques are employed to protect the upset-sensitive nodes of the circuit avoiding any loss of area. The area of one register is 14.6 × 3.6 μm², about twice the area of a standard D-FF, giving a storage density of 19 kbit/mm².

Heavily ionizing particles traversing an IC deposit most of their energy in the first few microns of trajectory in silicon. In this work the internal nodes of a bank of two registers are interleaved in order to reach a distance between correlated nodes of at least 4.5 μm. This distance is sufficient for the particle spectra present in the LHC experiment environment to avoid double-node hits on the register circuit.

The register circuit proposed was designed in a CMOS 130 nm technology, and fabricated in a test chip containing a shift-register of 4096 cells.

Test chips were irradiated in a heavy-ion beam facility in order to assess the register SEU tolerance. The shift-register was irradiated while running at 30 MHz clock frequency. The register showed a 1000 times soft-error rate improvement over a standard library register available in the same technology previously tested in the same facility. No soft-errors were observed in our register below an LET of 30 MeVcm²/mg. At higher LETs few soft-errors were recorded, giving a cross-section lower than 1e-10 cm²/bit.

Irradiation test was conducted at two different orientations of the chip with respect to the beam in order to assess the sensitivity to multiple-node hits (tilted chip and beam transverse/normal to standard cell rows). No significant difference in the behavior of the circuit was found in the two orientations.

Results of total ionizing dose tests will also be presented.

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