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A 256 channel 8 bit current digitizer ASIC for the Belle-II PXD

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The international DEPFET collaboration is developing a low mass vertex detector (PXD)for the future BELLE-II experiment at the SuperKEKB particle accelerator in Japan.
The PXD is based on monolithic arrays of DEPFETs which are read out in a rolling shutter mode.
The Drain Current Digitizer ASIC (DCD-B) is used for reading out this detector matrix. It provides 256 channels of Analog-Digital converters with a resolution of 7-8 bits each, running at a conversion speed of 12.5 MHz.The chip design and first measurement results will be presented.

Summary

The international DEPFET collaboration is developing a silicon pixel vertex detector (PXD), based on monolithic arrays of DEPFET transistors, for the future physics experiment BELLE-II at the SuperKEKB particle accelerator in Japan. The matrix elements are read out in a 'rolling shutter mode', i. e. rows are selected consecutively and all columns are read out in each cycle of <100ns. Therefore, as one of the major parts in the front-end electronics chain, the Drain Current Digitizer ASIC (DCD-B) is used. It is now in a close-to-final state. The chip provides 256 channels of Analog-Digital converters with a resolution of 7-8 bits. Each converter features an individual dynamic offset correction circuit as well as programmable gain and bandwidth. Several operation modes using single sampling or double correlated sampling are possible. A large synthesized digital block is used for decoding and derandomization of the conversion results. The data is sent out on eight 8 bit links, operating with a speed of 400MHz. Additionally, a JTAG compatible interface is implemented for configuration and debugging purpose. Significant effort was made reducing the power consumption of the DCD-B, since both, voltage drop on the internal power buses and heat sources in the BELLE-II experiment are a concern. The chip was realized on a 3.2mm x 5mm die using the UMC 180nm CMOS technology in a multi-project run provided by EuroPractice. An extra redistribution metal layer with solder bump bond pads is used, allowing for flipping the chip onto the final all-silicon DEPFET sensor module.
Several tests have been performed in order to demonstrate the chip's operation and it's quality in terms of noise. The results will be presented.

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