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Single Event Effect mitigation in digital integrated circuits for space

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Integrated circuits (IC) used in a space environment are exposed to solar and cosmic radiation, causing several adverse effects in the IC. Total Ionising Dose (TID) effects may lead to threshold voltage shift, increased leakage currents and reduced circuit speed. With advanced (deep-) sub-micron technologies, TID is of decreasing concern for most of the space applications (˜ 100 krad) and might not need special mitigation. For certain long-duration deep-space missions however, exposed to doses in the Mrad domain, the dose effects are mitigated by adequate transistor geometries and guard-rings in library cells, and by taking sufficient design margins (derating), anticipating the end-of-life degradation.

The main focus of this presentation is on how to protect space IC's against the second group of radiation effects, called Single Event Effects (SEE), which are caused by the interaction of (heavy) ions with the semiconductor material, generating electron-hole pairs leading to voltage peaks (glitches) within the drains of CMOS transistors. With decreasing capacitance of circuit nodes in advanced technologies, the SEE sensitivity increases. Depending on where in the circuit these glitches occur, the SEE can result in latch-up (SEL), transient pulses (SET) or bit upsets (SEU).

SEU hardening design techniques usually involves some form of redundancy. The redundancy can take different forms, for example triple redundancy and voting at bit-level or error correcting codes (BCH/Hamming/Reed-Solomon). SET hardening is usually done by increasing buffer sizes and node capacitances or by temporal filtering. These modifications can be introduced at different levels of the design, at transistor, gate/flip-flop level implemented within a standard cell ASIC library, in the gate-level netlist, during place & route of an FPGA, in the HDL code, at the level of sub-blocks of an IC or even of complete IC's. The choice of the right method and degree of protection is one of the main concerns in space IC design. It depends on the IC technology (e.g. FPGA, standard cell ASIC) and very largely on the requirements, the requested degree of robustness. Not all circuits need to be 100% error free, and overdoing protection can be detrimental to the main goal of an IC, to fulfil its functional requirement within a given area and power budget. This is why a sound radiation assurance approach is required: at first specify requirements, investigate technology capabilities, define the radiation hardening strategy, calculate/validate the error rate.

In many cases, adding redundancy contradicts the optimisation goals of commercial Electronic Design Automation (EDA) tools which were designed to avoid or remove redundancy, trying to select the smallest structure fulfilling a certain functional specification. Very often, specific tool set-ups or hand editing are required to produce a functional and rad-hard circuit.

The effectiveness of the radiation mitigation has to be proven before the IC is manufactured and launched to space. Before manufacturing, formal verification is employed to analyse the correctness of the redundancy on one hand, but also to verify that the circuit retains its functionality after adding the hardening 'features'. Fault simulation or fault emulation on FPGA prototypes can be applied. After manufacturing, earth-based radiation testing in particle accelerators are performed.

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