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High speed data transfer with FPGAs and QSFP+ modules

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We present test results and characterization of a data transmission system based on a last generation FPGA and a commercial QSFP+ module.
QSFP+ standard defines a hot-pluggable transceiver available in copper or optical cable assemblies for an aggregated bandwidth of up to 40 Gbps.
We implemented a complete testbench based on a commercial development card mounting an Altera Stratix IV FPGA with 24 serdes at 8.5 Gbps, together with a custom mezzanine hosting three QSFP+ modules.
We characterize all parts of this tranmission system with signal integrity, bit error rate and jitter measurements at different data rates and cables lenghts.

Summary

High speed data transfer will play a central role in trigger and data acquisition systems for future particle and astroparticle physics experiments (sLHC, ILC, CLIC, rare kaon decays). We present test results and characterization of a data transmis
sion system based on a last generation FPGA serializer driving an external commercial QSFP+ module.
QSFP+ is the evolution of the widely used SFP+ standard. SFP+ is an electrical and mechanical standard for point-to-point links over copper or optical fibers with data rate up to 10 Gbps. The QSFP+ (Quad SFP+) standard specifies a hot-pluggable transceiver that integrates 4 transmit and 4 receive channels for an aggregated bandwidth of up to 40 Gbps per direction. Together with high speed data rate, this technology is intended for high-density and low-power applications and is compatible with passive copper and active optical modules. The application using a QSFP+ module should provide data serialization and deserialization.
We implemented a complete test bench based on: a commercial development card mounting an FPGA with embedded high-speed serializer/deserializer, a custom PCI form factor mezzanine card hosting up to three QSFP+ connectors, some optical and electrical QSFP+ transceivers with different cable and fiber lengths.
The commercial development board mounts a last generation Stratix IV programmable device with up to 230k Logic Elements and 24 serdes up to 8.5 Gbps per channel. The FPGA implements all the serialization and deserialization for the QSFP+ modules an
d all the PCI Express Gen 2.0 x8 protocol. The board is plugged in a high-end commercial PC running standard linux. The configuration, data read and write from and to the QSFP+ modules are performed via the linux PC. The custom QSFP+ mezzanine is connected to the development card via 19 mm height high speed (11 Gbps) differentrial connectors.
A custom linux driver has been designed for this application.
We characterize all parts of our transmission system (transmission lines, connectors, cables) from the signal integrity point of view. Then we characterize the throughput, latency, bit error rate and jitter of the link at different data rates with optical and electrical cables of different lengths. Long data transfer tests between two PCs connected by this QSFP+ transmission system are also performed.

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