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Reliability and Performance Studies of DC-DC Conversion Powering Scheme for the CMS Pixel Tracker at SLHC

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The upgrades of the Large Hadron Collider (LHC) introduce a significant challenge to the power distribution of the detectors. DC-DC conversion is the preferred powering scheme proposed to be integrated for the CMS tracker to deliver high input voltage levels and performing a step-down conversion nearby the detector modules. In this work, we investigate the integrity of power distribution and perform pixel performance analysis using the DC-DC conversion powering scheme. Tests are performed using the PSI46 pixel readout chips on a forward tracker panel module and the AMIS2 DC-DC converters developed at CERN. Reliability studies include the voltage drop measurements on the readout chips and the power supply noise generated from the converter. Performance studies include pixel noise and threshold dispersion results. Additionally, we describe SPICE-level converter and readout chip models for simulation that quantify the voltage drop and power supply noise on the system.

Summary

The Electronic Systems Engineering (ESE) Department of the Computing Division at the Fermi National Accelerator Laboratory is carrying out R&D investigations for the upgrade of the power distribution system of the Compact Muon Solenoid (CMS) Pixel Tracker at the Large Hadron Collider (LHC). DC-DC conversion is the preferred powering scheme proposed for the CMS upgrade pixel detectors. This scheme enables the delivery of high voltage with low currents such that the voltage drop on the power cables is reduced. In this work, we provide an in-depth study of the DC-DC powering scheme by investigating the power integrity of the system and pixel performance for the forward tracker panel module.

The test stand is a forward tracker panel module which has 21 PSI46 pixel readout chips (ROCs). The DC-DC converters utilized are AMIS2 chips which are non rad-hard buck converters developed at CERN. The printed circuit board where the converter chip resides on is developed at RWTH Aachen. We utilize DC-DC converters to provide the analog and digital power to the panel module. We utilize the CAPTAN data acquisition system that was developed internally by our ESE team. The CAPTAN system enables the interface to the panel module where commands can be issued through the FPGA chip residing on the CAPTAN board. The gigabit Ethernet link (GEL) enables the communication from the user interface window (GUI) on the PC to the CAPTAN. In this fashion, we are able to issue commands i.e. to set ADC registers for the ROCs in the panel module. Such interface, also allows us to visually display pixel hits.

The objective of this work is to test the DC-DC powering scheme in the real detector environment. To power up the converter, we utilize the CAEN power supply and the multi-service cables (MSC) which are also used to power the pixel modules in the CMS detector. For cooling the panel module, we utilize a chiller box which can reach down to 2°C temperature.

We perform pixel performance analysis to capture the impact that the DC-DC powering scheme poses on the pixels. Power supply noise can cause performance degradation of the pixel readout chips. Therefore, we investigate the panel module when powered with and without DC-DC converters to derive the effect on the pixel performance. The parameters for measuring the impact of the power supply noise on the pixel performance are pixel noise and threshold dispersion variations. These measurements are re-performed and compared with the case when cooling is applied to the panel module and converter. Additionally, we study the possible impact of the power supply during the configuration and tuning of the pixel readout chip settings.

In this work, we also provide SPICE models for the DC-DC converter and readout chips for simulation purposes. Utilizing these models, we can perform power analysis studies at a system level to obtain the voltage drop and power supply noise of the readout chips.

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