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Design and Verification of a Bit Error Rate Tester in Altera FPGA for Optical Link Developments

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This paper presents a Bit Error Rate (BER) Tester implemented in an Altera Stratix II GX signal integrity development kit. Architecture of the tester is described. Experimental and simulation results are discussed.
A parallel to serial PRBS generator and a bit/link status error detector are deployed to characterize serial data link performance. The auto-correlation pattern enables receiver synchronization without specifying protocol at the physical layer. An error logging FIFO records both bit error data and link operation events. An optimization scheme is established to maximize throughput with shortest dead time. The tester operates up to 6.5 Gbps in 4 duplex channels.

Summary

Multi-gigabit per second optical links are widely conceived to support data transmission in future particle physics experiments. In order to qualify components and verify link designs, their performances need to be evaluated in the laboratory and sometimes in a radiation environment. Bit Error Rate (BER) testing is the fundamental measure of the integrity of each digital communication link. It traditionally requires expensive equipment with table-top testers. With the integration of high-speed SERDES inside FPGA, the embedded solution provides a cheaper alternative with the flexibility of customization to fit field irradiation test scenarios.

We develop a Bit Error Rate Tester (BERT) implemented in an Altera Stratix II GX signal integrity development kit. The tester includes VHDL codes and LabVIEW VIs. The former govern the data flow functions and the transceiver hardware. The latter provides user GUI and remote access of test operation. The main blocks of the VHDL codes are pattern generators, transceiver controls, error detector, link status monitor, and error logger. A Pseudo Random Bit Sequence (PRBS) generator produces long stress patterns without using a lot of memory. The PRBS detector functions without needing the receiver to acquire boundary alignment. This enables the link re-establishment from transmitter or receiver separately, independent of protocol at the physical layer. An error logging FIFO records both bit error data and link operation events. The recorded time stamp and XOR pattern of received and expected data can reproduce transmitted and received data, given the pattern is a known PRBS. When a link-lost-event occurs, it is time stamped and logged. During the link lost event, bit error is not relevant and is not recorded. Instead the duration of the link-loss-event is measured. The LabVIEW VIs provide hardware GUI through periodic GUI refresh, write configuration and read data based upon event request.

The tester's functionality is validated on an optical transmission test bench. BER vs. receiver sensitivity are measured to emulate stressed test conditions. Data acquisition efficiency is crucial in irradiation test data collection. It depends on data volume, data rate, IO throughput and embedded memory size. Several test bench simulations are conducted to optimize data acquisition flow parameters. A matrix of data flow parameters and speed test results is generated for user reference. This tester will be used in a proton test on the LOCs1 serializer in June 2010.

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